Development of an RFSoC-Based Direct-Sampling RF Signal Acquisition System for Beam Diagnostics at KOMAC

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1. Introduction

The Korea Multi-purpose Accelerator Complex (KOMAC) operates a 100 MeV proton linear accelerator whose radio-frequency (RF) systems and beam position monitors (BPM) require accurate measurement of the amplitude and phase of 350 MHz signals. In conventional instrumentation, the RF signal is first down-converted to an intermediate frequency (IF) by an analog mixer driven by a local oscillator, and the IF signal is then digitized by a moderate-speed analog-to-digital converter (ADC). Although this architecture has been widely adopted, it introduces gain and phase drift originating from the analog mixing stage, channel-to-channel imbalance, and a hardware cost that scales with the number of measurement channels.

Recent RF System-on-Chip (RFSoC) devices integrate multi-gigasample ADCs, hardware digital down-converters (DDC), programmable logic, and an application processor within a single package [1,2]. Such devices make it feasible to sample the accelerator RF signal directly and to perform the down-conversion entirely in the digital domain. This work reports the development of an RFSoC-based direct-sampling acquisition system for BPM and low-level RF (LLRF) applications at KOMAC, together with its integration into the Experimental Physics and Industrial Control System (EPICS) used for machine operation.

2. System Configuration and Methods

2.1 Hardware Platform

The acquisition system is based on a Pentek Model 5950 (Quartz) board incorporating a Xilinx Zynq UltraScale+ RFSoC device. The board provides up to eight 16-bit ADC channels with a maximum sampling rate of 4 GSPS, a hardware DDC per channel, an on-board LMX2594 wideband PLL synthesizer, and PCIe Gen3 x8 and 100 GbE interfaces. The processing system runs PetaLinux 2020.2 on an ARM Cortex-A53 (aarch64) processor, so that the acquisition and control-system software can be executed on the board itself. The principal operating parameters are summarized in Table I.

Table I: RFSoC acquisition system parameters

Parameter	**Value**
FPGA device	Zynq UltraScale+ RFSoC
ADC resolution	16 bit
Sampling rate	1 GSPS (max. 4 GSPS)
Input RF frequency	350 MHz (1st Nyquist zone)
Reference clock	40 MHz external, x25 via LMX2594
DDC decimation	1:8 (125 MSPS complex I/Q)
Channels acquired	4 of 8, externally triggered
DMA buffers	4 x 1 MiB per channel
Operating system	PetaLinux 2020.2, ARM Cortex-A53

2.2 Direct-Sampling Signal Chain

The 350 MHz accelerator RF signal is applied directly to the ADC input and sampled at 1 GSPS, so that the signal of interest lies within the first Nyquist zone and no analog mixer or IF stage is required. The ADC sampling clock is synthesized by the on-board LMX2594 PLL from the external 40 MHz machine reference with a feedback multiplication factor of 25, which preserves phase coherence between the digitized data and the accelerator timing system. Phase coherence obtained in this way is essential for BPM and LLRF measurements, in which the quantity of interest is the relative phase between channels rather than an absolute amplitude.

The numerically controlled oscillator of the hardware DDC is tuned to the signal frequency, and a decimation factor of eight is applied, producing complex in-phase and quadrature (I/Q) streams at 125 MSPS per channel. Amplitude and phase are then obtained from the I/Q pair without any further mixing operation. Because the down-conversion is performed inside the RFSoC, the analog front end is reduced to a band-limiting filter and an attenuator, and channel-to-channel imbalance arising from the analog stage is largely eliminated.

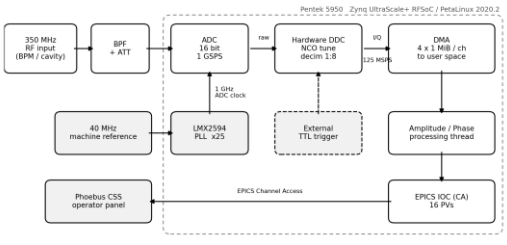


Fig. 1. Direct-sampling signal chain, from the 350 MHz RF input to the EPICS process variables.

2.3 Data Acquisition and EPICS Integration

Acquisition is initiated by an external TTL trigger. Decimated I/Q samples are transferred from the programmable logic to Linux user space by direct memory access (DMA), using four 1 MiB buffers per channel. The acquisition program was restructured as a three-stage pipeline: a DMA callback, a processing thread that computes amplitude and phase, and an EPICS Channel Access thread that publishes the results. Separating the callback from the later stages prevents the buffer overrun observed when the computation was performed inside the callback context at high trigger rates.

Sixteen process variables are exported, comprising scalar amplitude and phase values and the corresponding waveforms for each channel. They are displayed on a Phoebus CSS operator panel, so that the system is accessible from the existing KOMAC control network without additional middleware.

2.4 Runtime Bitstream Reconfiguration

To allow the signal-processing chain to be modified without interrupting board operation, runtime FPGA bitstream replacement was implemented. Two obstacles were resolved. First, the contiguous memory allocator was disabled in the vendor board support package kernel, so the kernel was rebuilt with a 512 MB region to enable the FPGA Manager interface. Second, the AXI interrupt controller registers are reset after a bitstream is reloaded, and the corresponding driver cannot re-probe because the node is defined in a static device tree. The registers are therefore restored through direct memory-mapped access after each reconfiguration, automatically by a startup script.

3. Results

Continuous externally triggered acquisition was verified with four channels operating simultaneously. Stable operation without data loss was confirmed at 333 Hz over extended runs, while the maximum rate sustained by the board was 487 Hz. Above this rate, message queue depth errors appeared in the DMA thread, indicating that the limit is imposed by the transfer and buffering path rather than by the ADC or the DDC.

Spectral verification was performed by comparing raw ADC captures with the decimated I/Q output. With the numerically controlled oscillator tuned to the input frequency, the down-converted spectrum shows its peak at baseband as expected. A decimation factor of eight was selected because smaller factors produce an integer relationship between the output sampling rate and the tuning frequency, folding spurious components onto the signal of interest.

Runtime bitstream replacement was exercised repeatedly on the operating board. After each replacement, interrupt delivery and DMA transfer resumed correctly following register restoration, and acquisition continued without rebooting.

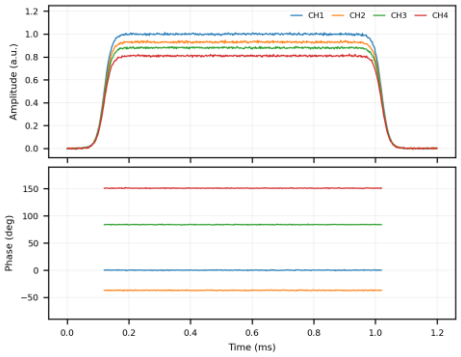


Fig. 2. Amplitude and phase of four channels reconstructed from the decimated I/Q streams at a 333 Hz trigger rate.

4. Conclusions

An RFSoC-based direct-sampling RF signal acquisition system was developed and evaluated for beam diagnostics at KOMAC. Sampling the 350 MHz RF signal directly at 1 GSPS and performing down-conversion in the hardware DDC removes the analog mixing stage entirely, while phase coherence is maintained by synthesizing the ADC clock from the external 40 MHz reference. The chain was integrated with EPICS and verified at a stable trigger rate of 333 Hz, and runtime reconfiguration of the programmable logic was demonstrated on the operating board.

Future work will address the transfer path that limits the trigger rate, extend the configuration to eight channels, and apply the platform to closed-loop LLRF measurement, where the reduction of analog drift is expected to be of direct benefit.

REFERENCES

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[2] Pentek Inc., Model 5950 Quartz RFSoC Transceiver, Product Datasheet.
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[4] EPICS, https://epics-controls.org.
[5] (KOMAC BPM / LLRF reference to be added.)