A Low-Area and High-Performance FPGA-based ENFMS using Fixed-Point Arithmetic

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1. Introduction

Reliable instrumentation and control (I&C) systems are essential for the safe operation of nuclear power plants. The Ex-core Neutron Flux Monitoring System (ENFMS) measures ex-core neutron flux in real time to support reactor operation. ENFMS must operate over an extremely wide reactor power range from 10^{-8} % to 10^{2} %, spanning the start-up, intermediate, and current ranges, based on the principle that leakage neutron flux is proportional to reactor power [1]. To achieve accurate measurement under this wide dynamic range, many FPGA-based ENFMS implementations rely on floating-point arithmetic, which increases DSP, Look-up Table(LUT), Flip-Flop(FF) utilization and accumulates latency in multi-stage pipelines. This paper replaces floating-point operations in the ENFMS signal processing chain with integer-based fixed-point arithmetic and optimizes bit precision using range-dependent scaling, enabling a low-area and high-performance FPGA implementation while preserving measurement accuracy.

2. Proposed Method

Figure 1 illustrates the block diagram of the digital ENFMS signal-processing unit [2]. The detector current is first combined into a single signal by a pulse accumulator and then processed by a CR–RC-based pulse-shaping filter to suppress noise and standardize pulse characteristics. After pulse shaping, the three measurement modes are computed in parallel. In the start-up range, the pulse mode output is valid because individual neutron pulses remain distinguishable, and reactor power is estimated by pulse counting. In the intermediate range, where pulse overlap increases, the MSV mode output becomes valid and reactor power is inferred from variance-related quantities. In the power range, where individual pulses are no longer separable and the signal approaches a quasi-continuous current, the current mode output is valid and reactor power is estimated from the mean current level. Finally, each mode output is converted by a logarithmic converter and, after interpolation, represented as a voltage in the range of 0 to 10 V. Among the arithmetic operations used in ENFMS, multiplication is one of the most frequently repeated and hardware-intensive operations. To illustrate the implementation difference between floating-point and fixed-point arithmetic, Fig. 2 shows an example comparison of multiplier architectures. In Fig. 2(a), the floating-point multiplier requires exponent processing, normalization, and exception handling in addition to multiplication, resulting in a multi-stage data path with substantial control logic [3]. This overhead typically increases LUT and FF utilization and pipeline latency, and may limit the achievable clock frequency on FPGAs. In Fig. 2(b), the fixed-point multiplier is implemented primarily as an integer multiplication followed by a scaling shift, resulting in significantly simpler datapath. Consequently, the fixed-point design generally achieves lower area and lower latency, while enabling a higher operating frequency and improved throughput.

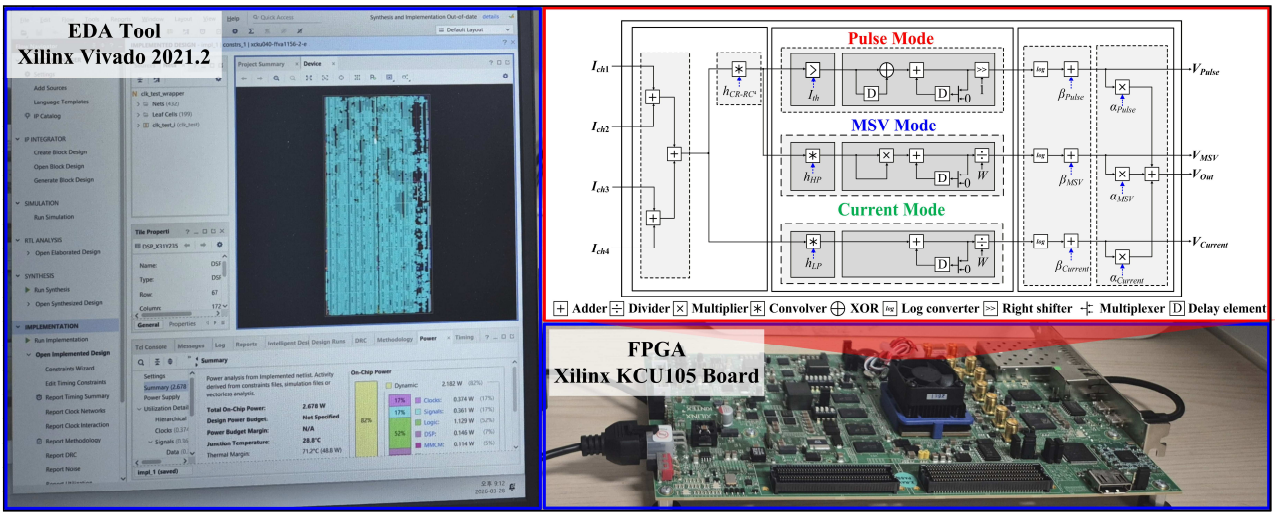

Fig. 1. FPGA based digital ENFMS platform and block diagram

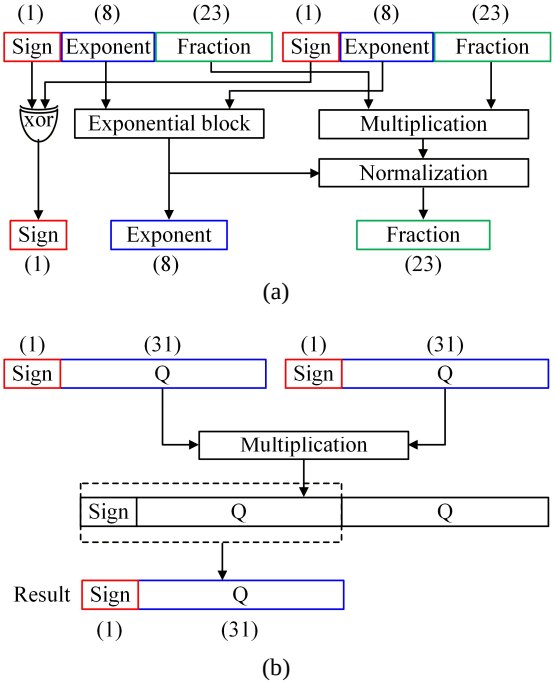

Fig. 2. Multiplier block diagram : (a) floating-point multiplier, (b) fixed-point multiplier.

Accordingly, this paper replaces floating-point arithmetic in the ENFMS processing blocks with fixed-point implementations, reducing hardware cost while maintaining the required measurement performance through stage-wise scaling. To minimize quantization error, bit sweeps are conducted for each processing stage, and the final bit width is determined as the minimum value that yields an RMSE of 0.001 or less, beyond which the improvement in accuracy becomes saturated, relative to the floating-point reference. Consequently, the proposed approach preserves the original signal processing functionality while improving implementation efficiency through operator-level simplification.

3. Experimental Results

The proposed ENFMS hardware is implemented on a Xilinx KCU105 FPGA board, and all designs are synthesized using Vivado 2021.2. For a fair comparison under maximum performance conditions, the floating-point based ENFMS and the proposed fixed-point based ENFMS are synthesized at their respective maximum achievable clock frequencies of 350 MHz and 450 MHz, respectively. Table 1 summarizes the synthesis results of the floating-point and fixed-point ENFMS architectures. Compared to the floating-point baseline, the proposed fixed-point design significantly reduces FPGA resource utilization. Using the slice-equivalent normalized area reported in Table 1, the fixed-point ENFMS achieves a 59.57 % reduction in area. Figure 3 compares the final ENFMS output signals generated by the floating-point and fixed-point implementations. Across operating modes, the fixed-point outputs closely match the floating-point reference, and the RMSE is below 0.01.

Table I. Implementation Results

	Floating-point ENFMS	**Fixed-point ENFMS**	**Improvement**
LUT	127,975	54,203	59.65 %
LUTRAM	75,276	28,635	61.96 %
FF	139,318	75,476	45.85 %
DSP	634	0	100.00 %
Area	**37,283.75**	**15,072.00**	**59.57 %**

*Area $= (\mathrm{LUT} + \mathrm{LUTRAM})/8 + \mathrm{FF}/16 + 5 \times \mathrm{DSP}$

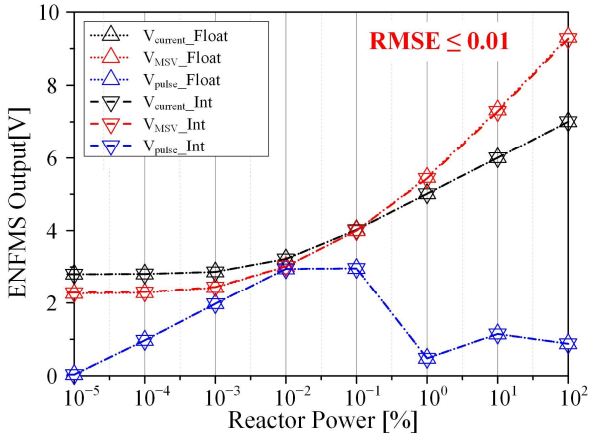

Fig. 3. Experimental Results.

These results confirm that the proposed fixed-point ENFMS preserves measurement accuracy while substantially reducing hardware cost and improving performance enabled by the higher operating frequency.

4. Conclusions

This paper presents a fixed-point FPGA implementation of a digital ENFMS by replacing floating-point operators in the signal-processing chain with integer-based fixed-point arithmetic. Implemented on a Xilinx KCU105 using Vivado 2021.2, the proposed design reduces the slice-equivalent normalized area by 59.57% and increases the maximum clock frequency from 350 MHz to 450 MHz compared with the floating-point baseline. The fixed-point outputs closely match the floating-point reference, and the RMSE is below 0.01, confirming that measurement accuracy is preserved while achieving lower area and higher throughput.

REFERENCES

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