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Design of a Parallelized Pulse Generation Algorithm

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1. Introduction

Small Modular Reactors (SMRs) are increasingly recognized as a next-generation nuclear technology amid global efforts to address climate change and achieve carbon neutrality [1]. SMRs enhance safety by integrating primary system components to reduce accident risks, while simultaneously offering economic efficiency through reduced construction and operational costs. The Korea Atomic Energy Research Institute, building upon its design experience with the SMART (System-integrated Modular Advanced ReacTor), is advancing the development of the innovative SMR (i-SMR).

The i-SMR is designed with lower reactor power and a dual containment structure, consisting of both the reactor vessel and containment vessel, compared to conventional nuclear power plants. Due to these design characteristics, the neutron flux leaking outside the containment vessel is expected to be very low, which may pose challenges for measurement. Consequently, the development of high-sensitivity detectors and advanced signal processing equipment is required to ensure reliable ex-core neutron flux monitoring under low-leakage conditions.

This study develops a hardware-based pulse signal generator utilizing Verilog. Given the extremely short generation time of a single pulse—typically on the nanosecond scale—high-speed signal processing is strictly required for real-time simulation [2, 3, 4]. Furthermore, the exponential increase in generated pulse signals corresponding to increasing reactor power necessitates parallel processing to accurately simulate the pulse pile-up phenomenon. Field-Programmable Gate Arrays (FPGAs) provide hardware-level parallelism, enabling significant improvements in computational performance.

This paper proposes a parallelization methodology for single-pulse signals, presents signal generation results across key operating intervals, and shows the hardware resource utilization of the parallelized implementation.

2. Design of the Parallelized Pulse Generation Algorithm

This section details the design of a parallelized architecture engineered to simulate neutron and gamma pulses.

2.1 Hardware-Optimized Parallel Algorithm

Hardware Description Languages (HDLs) like Verilog differ from traditional sequential programming. The concurrent execution model of HDL is implemented with algorithms optimized for hardware-level spatial synthesis rather than temporal instruction execution.

Fig. 1 illustrates the proposed algorithm, which is structured to distribute computational loads and simulate pulse pile-up phenomena to cover a wide range (Conventional plant range: 2e-8% ~ 200% ≈ 0.1 ~ 10^9 Counts Per Second (CPS)) [5].

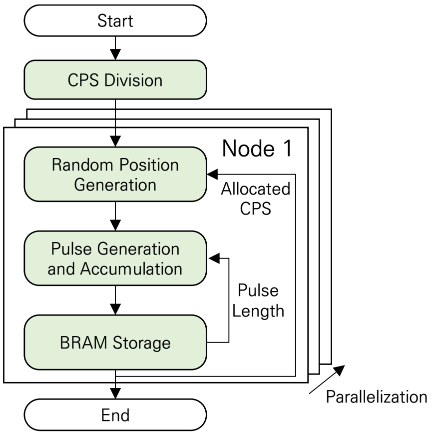

Fig. 1. Parallelized pulse generation algorithm

This algorithm is designed to overcome the sequential bottlenecks inherent in conventional software(e.g., Python). To simulate neutron and gamma pulses, the proposed framework comprises CPS division, a random pulse position generator, single-pulse generation and accumulation, and block memory storage.

In CPS division, the target total CPS is divided and allocated across multiple independent computational nodes. This parallel distribution mitigates the exponentially increasing pulse generation load associated with increasing reactor power. Then, each node iteratively executes the following sequence corresponding to its assigned CPS.

At each node, a single pulse is generated through a three-stage process. First, in the random position generation stage, a Linear Feedback Shift Register (LFSR) probabilistically determines the random start time of the pulse. Since the LFSR provides only simple randomness, the logic needs to be modified to follow a Poisson distribution to represent the physical characteristics of neutron signals.

Next, during the pulse generation and accumulation stage, a half-Gaussian pulse is generated over the predefined pulse length interval. The computed amplitude values are accumulated at every clock cycle using a read-modify-write operation with the existing signal values stored in Block RAM (BRAM). To realize the multi-pulse pile-up phenomenon at the hardware level, accumulation is performed sequentially from the pulse start position across the entire pulse length interval.

3. FPGA implementation & Results

3.1 Hardware Resource Utilization

The proposed signal generator was implemented on a Digilent Zybo Z7-20 board with a Xilinx Zynq-7000 SoC, and synthesized using the Vivado Design Suite. To assess the hardware portability and spatial efficiency of the proposed parallel algorithm, the post-synthesis resource utilization was systematically analyzed. Resource analysis necessary for implementing FPGA hardware was performed based on the algorithms of each of the above components established for digital signal processing [6]. Table 1 delineates the hardware mapping results and the utilization percentage of each primary resource within the ZyBo board environment.

Table 1: Hardware resource utilization

Number of node	Resource	Utilization	Available	Utilization [%]
1 Node	LUT (Look-Up Table)	2,210	53,200	4.15%
	LUTRAM	274	17,400	6.39%
	FF (Flip-Flop)	2,602	106,400	2.44%
	BRAM (Block RAM)	2	140	1.42%
	BUFG (Global Buffer)	1	32	3.13%
4 Node	LUT(Look-Up Table)	8,720	53,200	16.39%
	LUTRAM	1,112	17,400	6.39%
	FF (Flip-Flop)	8,946	106,400	8.41%
	BRAM (Block RAM)	9	140	6.43%
	BUFG (Global Buffer)	1	32	3.13%

The single-node pulse generation module was observed to consume less than 5% of the total resources on the ZyBo board. Furthermore, even with the implementation of a four-node parallel processing scheme, the maximum overall hardware resource utilization remained strictly below 16.39% (governed by LUT usage). Such low resource occupancy demonstrates the efficiency of the proposed algorithm at the hardware level. Arithmetically, maximizing the utilization of available hardware resources allows for the integration of up to 24 nodes within the same ZyBo board. In a parallel architecture, the total computation time scales inversely with the number of parallel nodes. Consequently, deploying a configuration of 12 neutron nodes and 12 gamma nodes operating concurrently is projected to reduce the total computation time to 1/24 of that required by a single-node setup.

3.2 Pulse Signal Simulation Results

Simulations were performed to test the pulse simulation performance of the proposed FPGA-based parallel architecture. Fig. 2 shows the pulse signal waveforms generated at 1.49e+5 CPS and 1.00e+6 CPS. This range corresponds to a critical crossover region in ex-core neutron flux monitoring systems, where the measurement mode transitions between operational regimes.

The simulation results show that the waveform at 1.49e+5 CPS partially preserves the individual semi-Gaussian pulse shapes while clearly exhibiting the onset of pile-up phenomena. In contrast, the waveform at 1.00e+6 CPS shows severe pulse superposition, resulting in an elevated signal baseline and continuous fluctuations characteristic of the Campbelling and current modes.

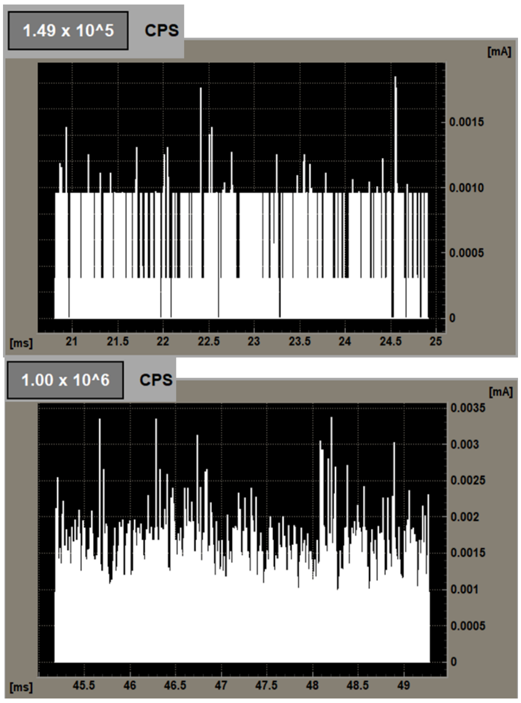

Fig. 2. Simulated pulse signal waveforms (1.49e+5 CPS, 1.00e+6 CPS)

6. Conclusions

This study developed an FPGA-based parallel pulse generation algorithm implemented in Verilog to simulate neutron and gamma pulses. By employing a hardware-optimized multi-node parallel processing architecture, the proposed simulator successfully reproduced both single-pulse behavior and pulse pile-up phenomena. However, the study remains at the simulation level. For practical deployment in real-world systems, analog signal conversion techniques are required, necessitating the use of a high-performance FPGA board.

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