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Characterization of Neutron-Induced Displacement Damage Mechanisms and Leakage Current Degradation in Si MOSFETs

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1. Introduction

In recent years, the adoption of semiconductor-based devices in nuclear applications has expanded significantly, driven by the digital transformation of instrumentation and control (I&C) systems. This trend is particularly evident in the transition toward Small Modular Reactors (SMRs) and micro-reactors, where the reduction in plant scale necessitates the placement of electronic components in closer proximity to the reactor core. Among various semiconductor technologies, CMOS-based MOSFETs constitute the vast majority of these systems due to their high integration density and low power consumption.

However, exposure to intense neutron radiation fundamentally compromises device reliability through displacement damage (DD). Unlike ionizing radiation, neutrons interact with the device through non-ionizing collisions, where the momentum transfer directly induces displacement damage in both the silicon bulk and the gate oxide layers [1]. These collision-induced defects serve as immediate sources of electrical degradation: within the silicon lattice, they act as efficient generation centers that elevate the leakage current via enhanced carrier generation. Simultaneously, displacement events occurring within or near the gate oxide (SiO2) introduce trapped charges and interface states, leading to a significant threshold voltage (V_{th}) shift.

Therefore, this paper systematically characterizes and validates the impact of neutron-induced displacement damage on CMOS MOSFETs, specifically focusing on the influence of different transistor structures. By evaluating the correlation between device geometry and radiation-induced degradation—such as carrier generation and threshold voltage shifts—this study aims to elucidate the underlying physical mechanisms that govern the reliability of CMOS electronics in neutron-rich environments.

2. Experimental Setup

2.1 Transistor Array with Geometric Variations

In this study, MOSFETs with varying geometric parameters were designed and fabricated as the devices

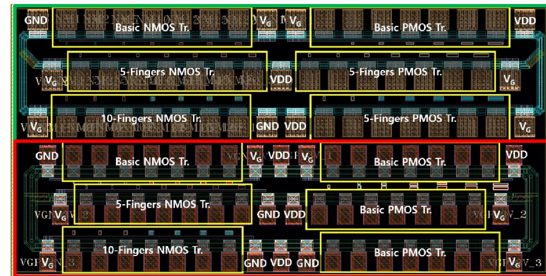

Fig. 1. Layout of the transistor array including 1.8V/3.3V NMOS/PMOS with variations in channel width and number of fingers.

under test (DUT) to systematically analyze the impact of neutron-induced displacement damage on electrical characteristics. The primary focus is to evaluate the structural dependency of neutron-induced leakage current enhancement and threshold voltage shift by investigating variations in channel width and gate oxide thickness [2].

The test samples consist of both NMOS and PMOS transistors designed for Core 1.8V and 3.3V operations, which allows for a comparative analysis based on different oxide thicknesses. To evaluate the geometric dependency of displacement damage, the devices were configured with a 7-step incremental variation in channel width. Furthermore, to analyze the impact of layout topology, a multi-finger structure was adopted with three different configurations 1, 5, and 10 fingers for each W variation.

As illustrated in Fig. 1, these diverse transistor combinations were monolithically integrated into a single-chip array. This design approach ensures uniform process conditions across all test cases and enables a high-precision characterization of the correlation between device architecture and radiation-induced degradation. The combination of finger count and channel width determines the ratio between the bulk volume and the junction area, serving as a critical variable for analyzing the "geometric density" of carrier generation that contributes to the off-state leakage current. Simultaneously, the dual-voltage (1.8V/3.3V) device set enables the independent extraction of how neutron-induced oxide traps and interface states affect V_{th} stability across different oxide regimes.

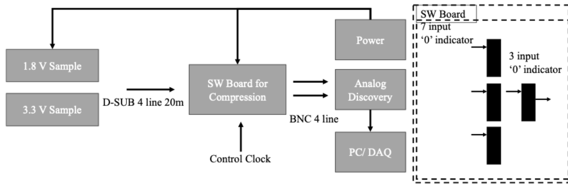

Fig. 2 . Schematic of the readout circuitry including the hierarchical 1 GHz multiplexing decoders for 84-channel data acquisition.

2.2 Readout Circuitry Configuration

To efficiently collect signals from the extensive transistor array during neutron irradiation, a specialized readout interface was developed. The array architecture features a common gate and 84 individual drain pads, posing a challenge for real-time data acquisition due to the limited number of high-speed measurement channels. To address this, a high-speed signal compression strategy was implemented as illustrated in the schematic in Fig. 2.

Each individual transistor within the array is configured as a Common Source (CS) Amplifier using an external load resistor. The circuitry is meticulously calibrated to operate at a stable common-mode voltage level, ensuring that variations in drain current due to displacement damage are accurately translated into voltage swings.

As shown in Fig. 2, the output signals from these 84 CS amplifiers undergo a two-stage hierarchical decoding process. First, the outputs are routed through 8x1 decoders operating at a high frequency of 1 GHz. These primary decoders sequentially sample the transistor outputs, with a '0' value inserted as an indicator to clearly delineate and synchronize individual data packets. Subsequently, these primary streams are grouped into three sets and processed through a second stage of decoders for final data collection. This architecture allows for the high-bandwidth, real-time monitoring of all 84 transistors through a significantly reduced number of output channels, which is critical for capturing transient and permanent degradation during neutron exposure.

2.3 Irradiation Conditions and Measurement Procedures

The neutron irradiation experiments were conducted at the TRIUMF cyclotron facility, utilizing the Neutron Irradiation Facility (NIF). Specifically, the Thermal Neutron Facility (TNF) and BL1B beamlines were employed to provide a characterized neutron spectrum. To analyze the degradation trends across varying exposure levels, the irradiation was performed in five incremental steps, covering a cumulative fluence range from 10^6 to 10^{10} n/cm^2.

During the irradiation process, a constant bias was applied to the DUTs to simulate realistic operating conditions and account for field-enhanced defect dynamics. The gate voltage was fixed at half-VDD, while the output signals from the transistor array were acquired in real-time through the high-speed readout circuitry described in Section 2.2.

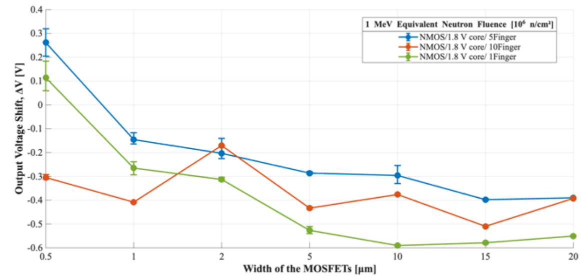

Fig. 3 . Measured output voltage shift of 1.8 V NMOS core devices as a function of channel width and finger configurations after neutron irradiation.

Furthermore, to investigate the long-term stability and defect recovery mechanisms, an extensive annealing study was performed. Following the final irradiation step, the electrical characteristics specifically the CS amplifier output voltage and threshold voltage were measured at periodic intervals: immediately after irradiation, and then at 1, 11, and 40 days post-exposure. This longitudinal tracking allows for a clear distinction between transient displacement effects and permanent lattice damage, providing critical insights into the stabilization process of neutron-induced defects in CMOS architectures.

3. Results and Analysis

The experimental analysis focused on the 1.8 V NMOS core devices to investigate the structural dependency of permanent degradation caused by DD. The output voltage (V_{out}) of the CS amplifier was measured under a constant gate bias of half-VDD.

As illustrated in Fig. 3, a distinct correlation was observed between the channel width (W) and the voltage drop ($\Delta V_{out} = V_{base} - V_{after}$) after irradiation. Specifically, as W increased, the magnitude of the output voltage reduction became significantly larger. Since V_{out} in a CS configuration is inversely proportional to the drain current, this drop indicates a permanent increase in the operating drain current due to DD-induced defects. This is attributed to the formation of stable generation centers within the silicon bulk a wider channel results in a larger total volume, increasing the probability of non-ionizing collisions and the subsequent density of these centers.

The layout topology also significantly influenced the results. The voltage reduction was more pronounced in 1-finger devices than in 5-finger devices, suggesting higher sensitivity in simpler geometries. Interestingly, the 10-finger devices exhibited an anomalous, non-linear trend that deviated from the linear scaling observed in 1 and 5-finger configurations. This suggests that in high-density multi-finger architectures, complex parasitic interactions or non-uniform damage distributions may dominate the degradation characteristics [4].

4. Conclusion

This study investigated neutron-induced DD in CMOS transistors using a 1 GHz single-chip array at the TRIUMF facility. For 1.8 V NMOS core devices, ΔV_{out} scaled with channel width, confirming a volume-dependent degradation mechanism. While 1-finger layouts showed higher sensitivity than 5-finger ones, 10-finger devices exhibited an anomalous non-linear trend. A more comprehensive analysis including 3.3 V I/O devices, NMOS/PMOS comparisons, and TCAD-based cross-validation of the 10-finger nonlinearity will be presented and discussed in detail at the upcoming conference.

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