

Design and Simulation of Auto-Frequency Tracking Digital LLRF Control Logic for Pulsed Operation of KAHIF RFQ

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1. Introduction

The Radio Frequency Quadrupole (RFQ) at the Korea Atomic Energy Research Institute Heavy-ion Irradiation Facility (KAHIF) plays a crucial role in accelerating various ion beams at an operating frequency of 25.96 MHz. Currently, the multi-stage vacuum tube RF system operates in pulsed mode with a legacy analog controller. This configuration faces two critical hardware challenges: 1) continuous thermal frequency shifts (std dev ~ 1.34 kHz) due to an out-of-service mechanical tuner (tuner-less condition), and 2) significant amplitude fluctuations (up to 3.7%) caused by initial transient delays and nonlinear pulse droops inherent to tube amplifiers.

To achieve high-quality beam dynamics, transitioning to a fully digital LLRF system is highly demanded [1]. The quantitative specifications required for the proposed digital LLRF architecture are defined in Table 1.

Table 1: LLRF Requirements

Parameter	Specification
Operating frequency	25.96 MHz
Frequency tuning range	$\geq \pm 10$ kHz
Amplitude stability	$< 1\%$
Phase stability	$< 1^\circ$
Operating mode	Pulsed mode
Control algorithm	AFC+PID

2. Proposed Digital LLRF Control Architecture

To satisfy the strict specifications without physical modifications, this study proposes a completely electronic Auto Frequency Control (AFC) combined with a Feedforward (FF) pulse control logic.

As illustrated in Fig. 1, the architecture consists of the following core digital loops:

- **DDC & AFC Loop:** The cavity pickup signals are directly demodulated into In-phase (I) and Quadrature (Q) baseband components [2]. The phase difference is calculated in real-time, allowing the Proportional-Integral (PI)

controller to dynamically adjust the Numerically Controlled Oscillator (NCO) frequency (Δf). This completely replaces the role of the physical tuner.

- **Feedforward-Combined Pulse Control:** To mitigate the sluggish response and droop of the vacuum tubes, pre-calculated Feedforward array values are injected at the onset of the pulse in parallel with the PID feedback compensation [3].

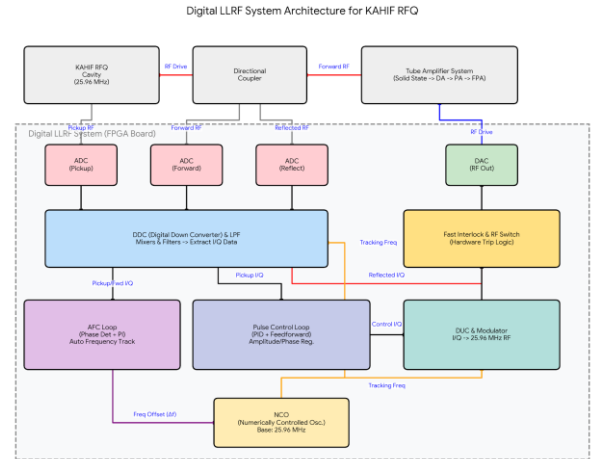


Fig. 1. Overall block diagram of the proposed digital LLRF architecture combining the purely electronic AFC loop and Feedforward-PID amplitude control.

3. Simulation Results

To verify the performance of the proposed digital algorithms, a time-domain simulation was conducted using MATLAB/Simulink.

3.1. Auto Frequency Control (AFC) Tracking Performance

A severe +10 kHz step frequency shift was intentionally injected to emulate extreme thermal deformation. As shown in Fig. 2(a), the PI controller successfully adjusted the NCO frequency offset to exactly +10 kHz instantly. Furthermore, Fig. 2(b) demonstrates that the demodulated I and Q amplitudes were maintained without long-term distortion, proving that the electronic AFC loop thoroughly satisfies the ± 10 kHz tuning requirement.

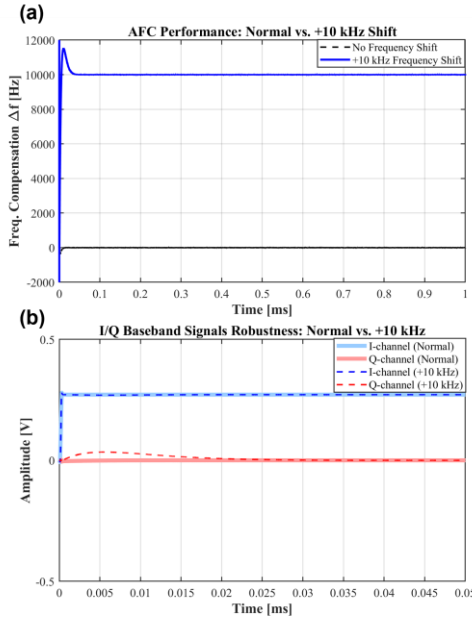


Fig. 2. AFC loop tracking response during a +10 kHz shift: (a) Frequency tracking, (b) I/Q baseband signals robustness.

3.2. Pulse Droop Compensation

To overcome the initial delay of the high-power vacuum tubes, a hybrid FF+FB amplitude control loop was simulated. As depicted in Fig. 3, the generated drive signal exhibits a sharp initial boost (FF component) at the onset of the pulse. This preemptive surge instantaneously charges the tube's parasitic capacitance, while the subsequent linearly increasing ramp (FB component) continuously compensates for the droop, effectively ensuring $< 1\%$ amplitude stability.

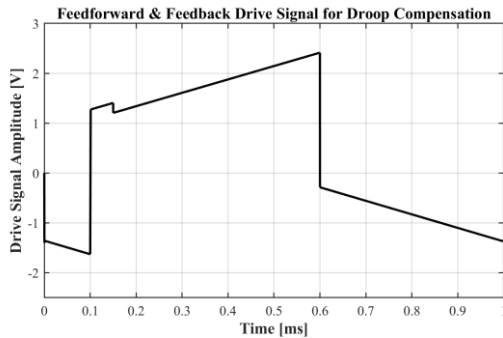


Fig. 3. Synthesized Feedforward (FF) & Feedback (FB) drive signal.

4. Conclusion

The digital LLRF control architecture was successfully designed and simulated for the tuner-less, tube-driven KAHIF RFQ. The electronic AFC loop demonstrated perfect frequency tracking up to ± 10 kHz, and the FF+FB hybrid loop effectively synthesized a droop-compensating drive signal. Future work will integrate a physical RLC equivalent model of the RFQ

cavity into the closed-loop simulation, followed by FPGA-based hardware implementation.

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