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Application-Specific SRAM for On-Chip Pixelized Histogramming in Multi-Channel Radiation Detectors

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1. Introduction

Conventional data acquisition (DAQ) systems for multi-channel radiation detection face critical limitations due to the high volume of raw data generated by dense readouts. This volume leads to severe off-chip data-rate bottlenecks, where the required throughput can exceed both the interface's physical limits and the system's power budget. As a result, lossless real-time streaming of full event data becomes difficult in practice. To overcome these issues, this research aims to design an on-chip pixelized HSRAM capable of performing cell-to-cell shift-based counting directly in memory. By mapping a hot-token ('logical 1') representing the accumulated count to an on-chip histogram bin per channel, the system streams only compact spectral histogram data rather than full raw event data, thereby achieving significant off-chip data-rate reduction and enabling real-time monitoring.

2. Proposed HSRAM Architecture

The proposed HSRAM is configured as a 4k-channel x 1k-bin array designed to maximize channel density and storage capacity within a limited silicon area. To achieve this, we propose a custom 9T SRAM bitcell, as shown in Fig. 1, that integrates a conventional 6T SRAM structure with a Static Sense-Amplifier Latch (SSALA) [1]. This 9T bitcell effectively implements a shift-register-based unary counter using pulsed latches. However, distinct from conventional long shift registers, where excessive delay circuits can cause timing overhead, we partition the count into M sub-shift registers, as illustrated in Fig. 2, to minimize the number of required delayed pulsed signals and dead time [2]. As demonstrated in low-power designs, the use of pulsed latches – enabled here by the SSALA configuration – significantly reduces transistor counts compared to standard flip-flops. This compact 9T cell structure allows the massive 4k-channel x 1k-bin array to be integrated efficiently. Furthermore, to mitigate RC delays in such a large array, we adopt a Hierarchical Subarray architecture [3]. By partitioning the array into Local Blocks (LBs), we decouple the local wordlines/bitlines from global interconnects, optimizing both writability and access speed.

3. Proposed Operation Scheme

3.1. Write Operation: Hot-Token Propagation & Activity Flagging

The counting mechanism is driven by a hot-token propagation scheme. When a radiation event occurs, a shift pulse is generated for the corresponding channel, shifting the hot-token to the next bit position within the 9T bitcell chain, as shown in Fig. 3. In this position-encoded counting scheme, the position of the hot-token directly represents the accumulated count value, eliminating the need for complex adder logic. Consequently, this approach bypasses the conventional multi-cycle read-modify-write process, enabling single-cycle count updates with minimized latency for simultaneous multi-channel counting.

Simultaneously with the counting step, an activity–sensitive flag latch is utilized within each local block. Specifically, the flag latch is coupled to the first bitcell of the block. Whenever the hot-token crosses the boundary into a new local block, this flag is triggered and set to a logic '1', as shown in Fig. 4. This operation serves as a critical pre-processing step for the subsequent readout phase, effectively marking the block as containing valid data.

3.2. Readout Operation: Sparse Readout & In-Memory Encoding

The readout architecture utilizes the previously set flag latches to eliminate unnecessary bitline switching power on empty blocks. The flag latch output is logically ANDed with global control signals to selectively activate local word and bitlines only when valid data exists, effectively isolating empty blocks. Consequently, this hierarchical decoupling primarily mitigates the excessive parasitic RC overhead that causes signal degradation in large-scale arrays, thereby ensuring robust readout reliability. As a secondary benefit, the reduced capacitance on local bitlines enables rapid voltage swings, enhancing the overall readout speed.

Furthermore, an In-Memory Binary Encoding scheme utilizing ten encoded lines is implemented. The active hot-cell directly drives specific lines corresponding to its column index, enabling contention-free, direct 10-bit binary readout without the need for peripheral encoders. Finally, the complete schematic of the local block, integrating the circuitry for both the write and readout operations, is illustrated in Fig. 5.

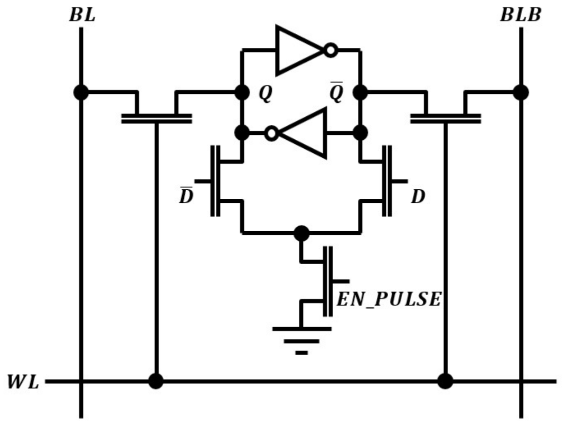


Fig. 1. Architecture of an HSRAM cell

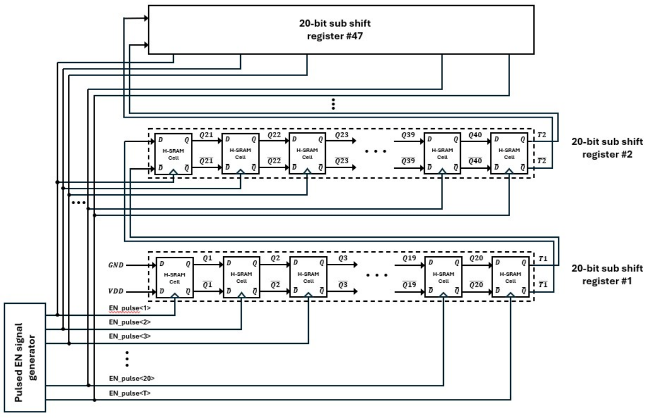
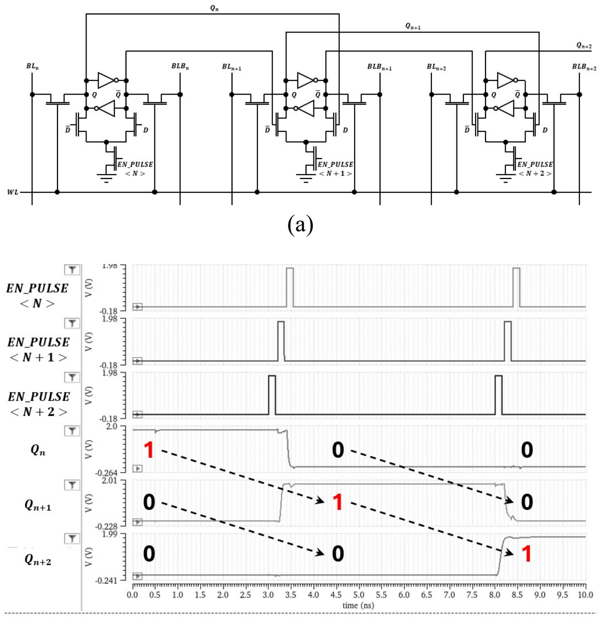


Fig. 2. Schematic of the proposed shift register



(a)

(b)

Fig. 3. HSRAM bitcells from n to n+2. (a) Schematic. (b) Waveforms.

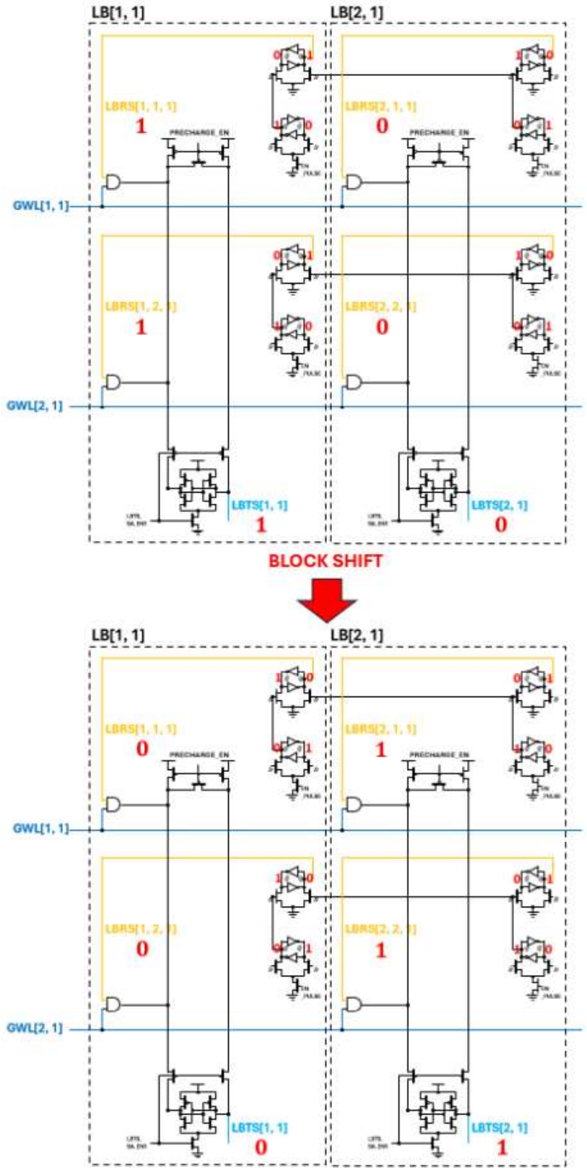


Fig. 4. Hot-token propagation across the LB boundary triggering the flag latch

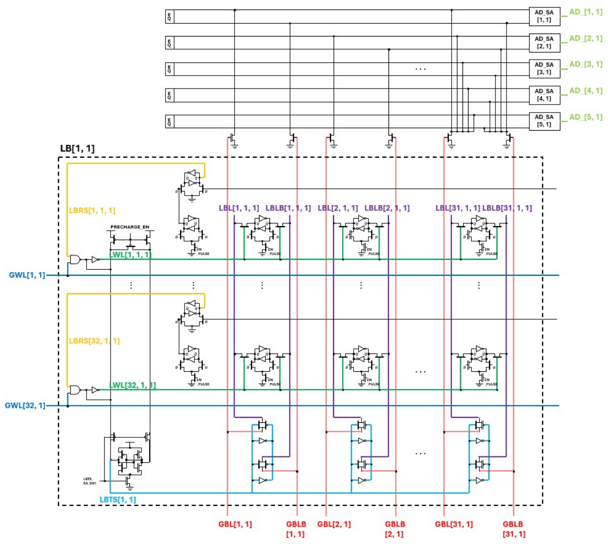


Fig. 5. Circuit diagram of a single LB in a divided subarray. (LB[a, b]: local block (a: block x index, b: block y index); GWL[a, b]: global wordline (a: local GWL index, b: local block row index); GBL[a, b]: global bitline (a: local GBL index, b: local block column index); LWL[a, b, c]: local wordline (a: local row index, b: block x index, c: block y index); LBL/LBLB[a, b, c]: local bitline/local bitline_bar (a: local column index, b: block x index, c: block y index); LBRS[a, b, c]: local block row select (a: block x index, b: block y index); AD[a, b]: address (a: local 5-bit address, b: local block column index)

4. Conclusion

This paper presents an HSRAM architecture optimized for high-density radiation detectors. By utilizing a custom 9T bitcell with SSALA-based pulsed latches, the design achieves the high integration density required for on-chip counting, enabling the direct formation of the expected on-chip pixelized histogram as illustrated in Fig. 6. The combination of hierarchical sparse readout and in-memory binary encoding effectively resolves the data bottleneck problem.

As summarized in Table 1, projected performance specifications indicate that the proposed HSRAM is expected to achieve a massive data reduction ratio of approximately 1,000 times that of conventional DAQ systems. Furthermore, the single-cycle in-memory counting operation targets an ultra-low energy consumption of less than 0.3 pJ per event, making it a highly viable solution for next-generation real-time radiation monitoring.

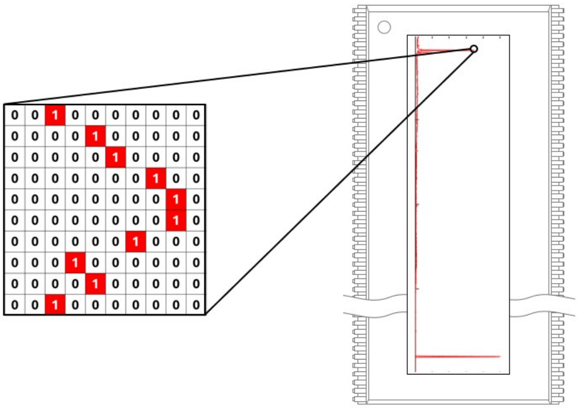


Fig. 6. Expected on-chip pixelized histogram

Table I. Comparison of Conventional Readout Architectures and Target Specifications of HSRAM

Feature	**Conventional DAQ**	**One Shared Adder + FPGA**	**HSRAM**
Average off-chip data rate	~ MB/s	~ kB/s	~ kB/s
Area	N/A	> 200 mm^2	~ 60 mm^2
Energy per event	0.1~1 nJ	10 ~ 100 pJ	< 0.3 pJ
Dead time	Multi-cycle (> 10 clks)	Multi-cycle (3 ~ 5 clks)	Single-cycle (1 clk)

5. Acknowledgement

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6. References

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