Design of FPGA-ADC Based Digital RF Interlock System for High-Power RF System at KOMAC 100MeV Proton LINAC

Young-Gi Song*, Hae-Seong Jung, Jae-Ha Kim, Sung-Yun Cho, Hyeok-Jung Kwon
Korea Atomic Energy Research Institute, KOMAC
181 Mirae-ro, Geoncheon-eup, Gyeongju-si, 38180, Republic of Korea
Corresponding author: ygsong@kaeri.re.kr

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1. Introduction

At KOMAC, 100MeV proton accelerator operates high-power RF systems to generate and sustain accelerating fields. Protecting these systems from reflected power, arcs, and vacuum degradation is critical for reliability and personnel safety. Interlock systems are designed to rapidly detect anomalies and shut down RF sources to prevent catastrophic failures.

Traditionally, analog-based interlock circuits have been employed due to their fast response [1]. However, analog solutions are inherently rigid, sensitive to drift, and incapable of providing post-event analysis. Recent advances in FPGA and ADC technology enable digital interlock systems that combine fast response with flexible reconfigurability. This paper presents the design of a digital RF interlock system using FPGA and ADC technology, integrated with EPICS-based control systems for accelerator applications.

2. System Requirements

The digital RF interlock system is designed to meet stringent performance requirements to ensure reliable operation of high-power RF components in particle accelerators. The ADC subsystem is required to support a unipolar input range of 0 to 5 V with a minimum resolution of 16 bits and a sampling rate of at least 1 MSps. Six independent analog input channels are provided via BNC connectors to allow simultaneous monitoring of multiple RF signals.

Trigger and digital I/O capabilities are essential for synchronizing waveform acquisition and interlock actions. The system implements two trigger inputs and two trigger outputs, all compatible with 3.3 V logic levels. Additionally, five digital input channels and five digital output channels (normally open relay type) are included to interface with external interlock and monitoring devices. The overall interlock latency must not exceed 20 μs to ensure fast response to abnormal conditions.

For communication and control integration, the system provides 1G Ethernet connectivity to support EPICS IOC operations, while an RS-232 UART interface allows debugging and console access. The processing platform is based on a Xilinx Zynq-7000 SoC [2], featuring an ARM Cortex-A9 processor for running the IOC and programmable logic for ADC data processing and interlock execution. DDR memory is incorporated for waveform storage and postmortem analysis.

Mechanically, the system is housed in a standard 19-inch, 1U rack-mount chassis. The production plan includes one prototype unit and nine operational units intended for deployment in accelerator facilities.

3. System Design

The high-frequency interlock system constitutes a critical safety infrastructure, designed not merely as a protective device but to concurrently ensure equipment protection, personnel safety, and operational stability. Consequently, such an interlock system must provide high reliability and rapid response, while offering real-time analysis of VSWR and arc detection from high-frequency signals. In this work, a digital RF interlock system is proposed, capable of storing and verifying current threshold values, as well as supporting real-time monitoring and recording of high-frequency power, thereby enhancing both operational safety and system diagnostics.

3.1 Architecture

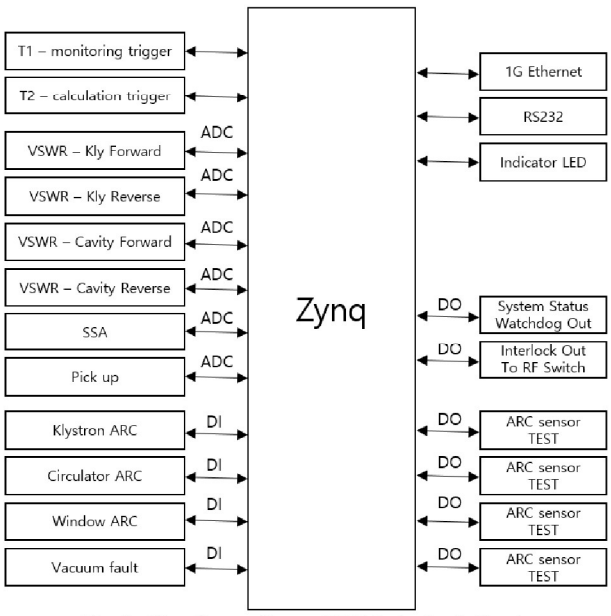

Fig 1. Configuration of RF Interlock System

The proposed device employs a six-channel ADC to continuously monitor the VSWR, while providing a digital input channel for high-frequency arc detection and a digital output channel for arc sensor testing as shown in Fig. 1. To enable stable operation of Zynq-based digital chips, the system output both a watchdog signal and an interlock signal to external devices. Moreover, a post-mortem function is embedded, enabling signal analysis at the moment of interlock events.

The RF Interlock Box receives analog RF signals from external devices, digitizes them via ADC, and performs real-time processing in FPGA logic. The FPGA calculates average values, evaluates polynomial equations up to 12th order, and determines interlock conditions. The processor system executes EPICS IOC [3], stores waveforms in DDR memory, and provides operator interfaces through Ethernet.

3.2 Trigger System Architecture

In the proposed control system, two independent trigger types are implemented to ensure both reliable monitoring and rapid protective actions.

Monitoring Trigger: This trigger is responsible for initiating waveform acquisition. It allows the system to capture and visualize signals for subsequent analysis without interfering with other critical operations. The primary purpose of the monitoring trigger is to support diagnostic and performance evaluation tasks, enabling detailed observation of system behavior.

Interlock Trigger: The interlock trigger is dedicated to real-time anomaly detection and safety mechanisms. Upon activation, it executes interlock logic and generates appropriate output responses to prevent potential system damage or unsafe operating conditions.

The separation of monitoring and interlock triggers ensures that the system can simultaneously perform continuous observation and implement protective actions as shown in Fig. 2. This dual-trigger approach prevents performance degradation that might otherwise occur if a single trigger were used for both monitoring and interlock functions. Consequently, the system maintains high reliability, rapid response, and robust operational safety.

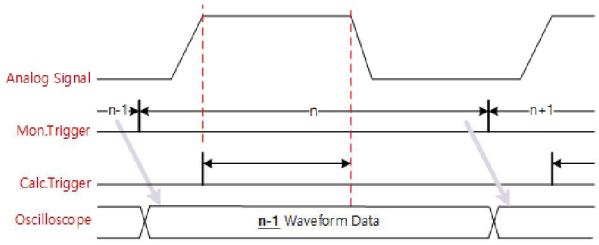

Fig 2. Trigger Timing of RF Interlock System

Two types of input triggers are implemented: one for ADC monitoring and another for interlock monitoring and computation, both operating independently. The ADC monitoring trigger captures data from all ADC channels immediately upon activation and stores it in the Zynq PS DDR memory for a user-configurable duration, primarily for graphing purposes.

The interlock monitoring and computation trigger is intended for precise analog signal measurement. Upon activation, the analog interlock is enabled, and real-time averaging of the ADC data is performed. After a user-defined interval, the averaging process and analog interlock are deactivated, and the resulting average is processed through a 12th-order equation to compute the corresponding power values. The computation must be completed before the next trigger occurs, with rapid data transmission, and a configurable delay following the trigger is also supported.

3.3 Interlock Logic

The interlock system implements a hierarchical, multi-level protection scheme to safeguard the RF components from abnormal operating conditions. The algorithm is structured into three distinct levels of response. Level 1 serves as an early warning mechanism: when monitored parameters such as forward power, reflected power, or cavity vacuum exceed predefined thresholds, a warning signal is generated and recorded, allowing operators to take preventive actions without immediately interrupting RF operation. Level 2 enforces a temporary RF mute, disabling RF drive to specific devices to prevent further stress or potential damage while the system continues to monitor conditions. Level 3 constitutes a full RF shutdown, where the FPGA triggers an immediate cessation of RF power to protect critical components from catastrophic failure.

The interlock logic is implemented entirely within the FPGA programmable logic, ensuring extremely fast response times. By processing ADC data in real time and continuously evaluating polynomial-based thresholds, the system achieves a total interlock latency of less than 20 μs. This latency is sufficiently short to respond to fast transients, such as arcs or rapid cavity reflections, providing robust protection that meets the demanding requirements of accelerator RF systems.

3.4 Control Integration

The processor system hosts an EPICS IOC, providing process variables (PVs) to the accelerator control room. Operators can remotely configure thresholds, monitor interlock states, and access stored waveforms for postmortem analysis.

4. Final Hardware Design

The final hardware implementation confirms the effectiveness of the proposed digital RF interlock system through both simulation and preliminary hardware testing. The ADC modules demonstrate a resolution exceeding 16 bits at a 1 MSps sampling rate, ensuring precise signal acquisition. The FPGA-based

interlock logic achieves a response time within 20 μs, providing rapid protection against potential faults. Communication with the EPICS IOC over Ethernet has been verified to be stable and reliable, supporting continuous monitoring and control.

Compared to conventional analog interlock systems, the digital design offers significant advantages. The system allows software-based adjustment of thresholds and processing algorithms, providing flexibility to adapt to different operational conditions. It also supports multi-channel monitoring with complex logic operations, enhancing scalability for larger or more intricate setups. Reliability is improved through digital filtering and robust FPGA logic, reducing susceptibility to noise and drift. Additionally, the system facilitates comprehensive diagnostics by enabling waveform recording and postmortem analysis, which aids in understanding and troubleshooting interlock events.

5. Conclusions

A digital RF interlock system based on FPGA and ADC technology has been designed for RF protection. The system meets strict latency and resolution requirements, integrates seamlessly with EPICS control systems, and supports advanced diagnostic features. This design addresses the shortcomings of analog systems and offers improved flexibility, reliability, and scalability for KOMAC facilities.

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