Development of FPGA Hardware for Real-time Neutron and Gamma Pulse Simulation

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1. Introduction

Small Modular Reactors (SMRs) are increasingly recognized as a next-generation nuclear technology amid global efforts to address climate change and achieve carbon neutrality [1]. SMRs enhance safety by integrating primary system components to reduce accident risks, while simultaneously offering economic efficiency through reduced construction and operational costs. The Korea Atomic Energy Research Institute, building upon its design experience with the SMART (System-integrated Modular Advanced ReacTor), is advancing the development of the innovative SMR (i-SMR).

The i-SMR is designed with lower reactor power and a dual containment structure, consisting of both the reactor vessel and containment vessel, compared to conventional nuclear power plants. Due to these design characteristics, the neutron flux leaking outside the containment vessel is expected to be very low, which may pose challenges for measurement. Consequently, the development of high-sensitivity detectors and advanced signal processing equipment to ensure reliable ex-core neutron flux monitoring under low-leakage conditions.

This study focuses on the development of an FPGA hardware for real-time neutron and gamma pulse simulation. The simulated signals reproduce both the semi-Gaussian pulse shapes of neutron and gamma ray and the associated pile-up phenomena, which are difficult to realize with conventional signal generators [2]. Field-Programmable Gate Array (FPGA) was employed to rapidly reproduce pulse generation and pile-up phenomena observed in neutron and gamma signals. Furthermore, the simulation should be designed with a wide dynamic range covering the typical ex-core detector operating range of conventional nuclear power plants (2×10^{-8} % to 2×10^{2} %)[3], with the intention of meeting the requirements of specialized reactor environments such as Small Modular Reactors (SMRs), which generally operate at lower power levels.

2. Design of FPGA Hardware

Fig. 1. illustrates the internal architecture of the FPGA hardware for simulation. On the PC side, the human–machine interface (HMI) allows the user to input the desired count per second (CPS) value. This CPS information is transmitted to the FPGA, where a random pulse start point generator initiates stochastic pulse events. The single pulse generator processes these events, and the resulting signals are shaped according to the neutron/gamma pulse profile. A floating-point adder combines the signals, which are then stored in block memory. Based on the input CPS, the FPGA calculates the corresponding pulse signals and transmits them back to the PC. The FPGA hardware is designed to generate continuous signals that dynamically respond to changes in the input CPS, thereby ensuring real-time operation and allowing subsequent conversion into analog pulse signals.

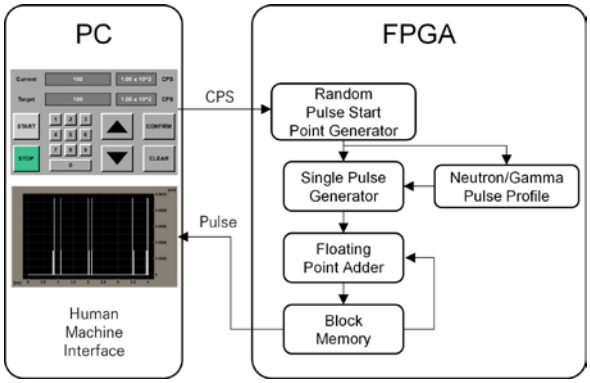

Fig. 1. Architecture of FPGA hardware for pulse simulation

2.1 Random Pulse Start Point Generator

To provide random pulse sequences, a linear feedback shift register (LFSR) was implemented within the FPGA. The LFSR generates pseudo-random binary sequences with a long periodicity, which are suitable for emulating the stochastic nature of neutron events. By exploiting its lightweight hardware complexity and high-speed operation, the LFSR ensures efficient generation of random start points for pulse events without imposing significant resource overhead.

In this study, a 10-bit LFSR was employed, taking into account the limitation of a single block memory in FPGA board (Zybo z7-20). The characteristic polynomial adopted for implementation is:

$$(1)\quad P(x) = x^{10} + x^{3} + 1$$

With a non-zero initial seed, the generated sequence achieves the maximal period of 1023, thereby providing sufficiently long pseudo-random patterns to emulate the stochastic behavior of neutron pulse events.

2.2 Single Pulse Generator

The Single Pulse Generator produces individual pulse signals based on the random onset times generated in the preceding stage. The pulse shape is determined by retrieving the corresponding values from the neutron/gamma pulse profile, thereby ensuring that each pulse reflects realistic detector response characteristics. Each generated pulse is represented as a pair consisting of its temporal position and amplitude value, and this structured output is subsequently transferred to the floating-point adder for accumulation with other pulses.

2.3 Floating-point Adder

The Floating-Point Adder is responsible for accumulating the outputs generated by the Single Pulse Generator. Each pulse is represented as a set of floating-point values, and since multiple pulses may temporally overlap, this module performs real-time summation of pulse amplitudes expressed in floating-point format. In this study, a 32-bit floating-point arithmetic unit was employed to ensure numerical precision, thereby enabling the generation of realistic neutron and gamma pulse signals.

2.4 Block Memory

The block memory is used as the storage unit for the accumulated pulse signals. The pulse signals summed by the Floating-Point Adder are written into the block memory in temporal order, which allows efficient storage and retrieval of composite pulse sequences. The stored data are subsequently transmitted to the PC via Ethernet communication, enabling high-speed data transfer and further processing outside the FPGA.

3. FPGA Implementation

The proposed pulse simulator was implemented on a Digilent Zybo Z7-20 board with a Xilinx Zynq-7000 SoC, and synthesized using the Vivado Design Suite. The overall architecture is shown in Fig. 2.

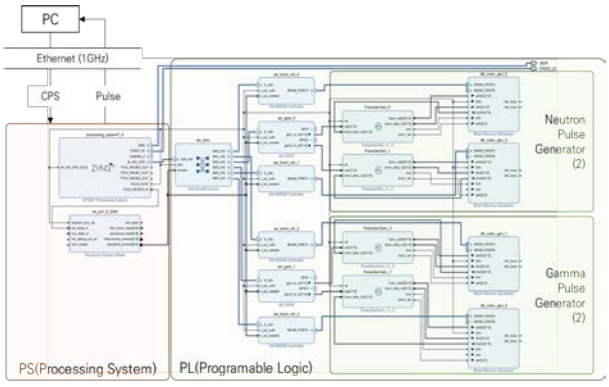

Fig. 2. Vivado block diagram of FPGA-based pulse simulator

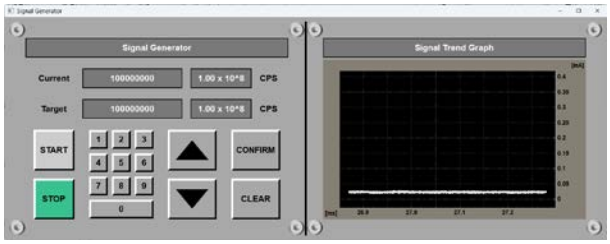

Fig. 3. Pulse simulation controller & monitoring interface

The processing system (PS) communicates with the PC via a 1-Gbps Ethernet interface, while the programmable logic (PL) hosts independent neutron and gamma pulse generator modules that employ random pulse start generation, floating-point addition, and block memory storage. The HMI was developed in Python 3.13.3 using PyQt5, enabling users to input and monitor CPS values in real time. As illustrated in Fig. 3, the interface provides start, stop, confirm, and clear functions, and displays the trend of the simulated signals for continuous signal monitoring.

4. Demonstration

Fig. 4. shows the experimental setup for performance evaluation of the neutron/gamma pulse signal simulator implemented on the FPGA board. The system stably simulated pulses across the full range from 1 to 10^9 CPS, with 32-bit floating-point arithmetic ensuring high precision and Ethernet communication providing reliable real-time monitoring.

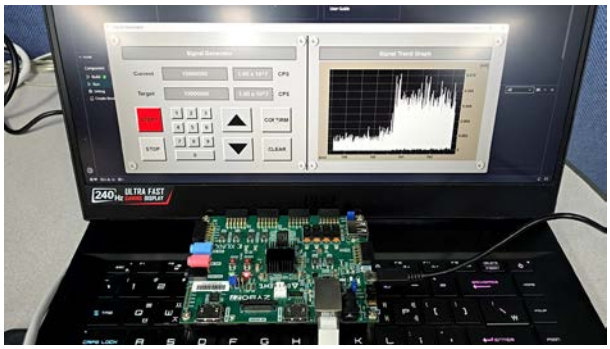

Fig. 4. Demonstration configuration

5. Discussion

The FPGA hardware developed in this study demonstrated combined signals of neutron and gamma pulses, but several limitations should be addressed to develop a practical test instrument. First, the FPGA hardware is a simplified prototype intended for demonstration and basic testing, and a digital-to-analog conversion (DAC) module is necessary for practical application. Second, although the FPGA hardware was designed for real-time signal simulation, the simulation speed decreases as the number of pulses increases. This issue arises from hardware constraints such as the

restricted operating frequency of 50 MHz, the limited 64 KB of BRAM, and the effective throughput of the 1-Gb Ethernet link being lower than the theoretical maximum during transmission. To resolve these bottlenecks, the adoption of a high-performance FPGA board, the integration of larger and faster memory resources, and the use of specialized IP cores for high-throughput data processing should be used.

6. Conclusions

In this study, an FPGA hardware for neutron/gamma pulse simulator was developed to remain applicable under varying ex-core neutron flux conditions in next-generation reactors such as SMRs. The proposed simulator successfully reproduced neutron and gamma pulse shapes, as well as pile-up phenomena, which are difficult to achieve with conventional analog signal generators. In the demonstration, the simulator showed stable and reliable signal generation across the output range relevant to commercial nuclear power plants.

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