Design of High Speed Digital Silicon Photo-Multiplier (SiPM) Using Common 180 nm CMOS Process

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1. Introduction

Optical measurement has been widely utilized across various research fields and plays a critical role in advanced industries. Consequently, the performance of optical measurement systems has rapidly evolved. Semiconductor-based silicon photomultipliers (SiPMs) have gained significant attention due to their high sensitivity in low-light environments, compatibility, and fast response time. Along with these advantages, the SiPM is extensively utilized in various fields, including Light Detection and Ranging (LiDAR), Fluorescence Lifetime Imaging Microscopy (FLIM), Raman spectroscopy, and optical communication. Additionally, it serves as a key component in radiation detectors for Positron Emission Tomography (PET) and radiation leakage measurement in nuclear power plants, with its applications continuously expanding.

While conventional analog signal processing based SiPMs retain these advantages, they exhibit inherent limitations in terms of noise, response time, and resolution. To address these challenges, extensive research has been conducted to enhance and refine SiPM technology. Among the various approaches, digital-SiPMs (d-SiPMs), which process signals by converting the output of individual avalanche photodiode (APD) pixels into digital signals, have emerged as a promising next-generation solution and are actively being investigated.

The d-SiPMs varies significantly depending on the type of signal and performance requirements [1]. Through direct integration, d-SiPMs can enhance the fill factor and enable complex on-chip processing. In a typical d-SiPM, single-photon avalanche diodes (SPADs) or Geiger-mode avalanche photodiodes (GM-APDs) are used for photon-to-signal conversion, with their performance varying greatly depending on the junction structure and node design. Time-to-digital converters (TDCs) or comparators are commonly employed to convert photon signals into digital signals. Additionally, active quenching circuits (AQCs) are often integrated to optimize performance by controlling SPAD operation. AQCs effectively regulate the quenching, hold-off, and reset states of SPADs, thereby minimizing dead time while suppressing dark count increases and mitigating afterpulsing effects. The signals generated by each pixel are subsequently compressed and processed or preprocessed according to the intended application. Since d-SiPMs process digital signals, they offer advantages such as low jitter, fast response time, and strong immunity to noise that may arise during the readout process.

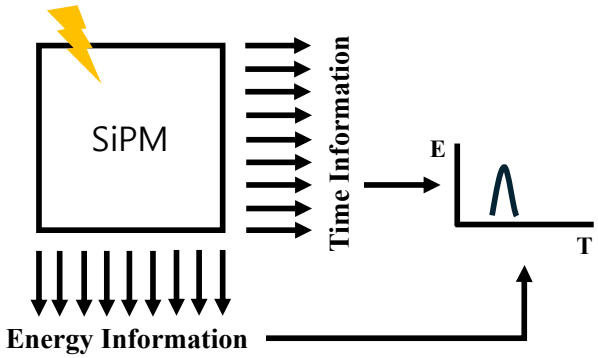

Fig. 1. The function diagram of the SiPM as a type of output signals.

Overall, d-SiPMs exhibit more advanced characteristics than conventional SiPMs; however, certain aspects still require improvement. Optimizing SPAD operation at the pixel level and minimizing signal loss during the compression process remain key challenges [2]. SPAD operation can be refined by characterizing individual SPADs to optimize hold-off time and reset time, while quenching circuit design enables control over output magnitude. Given that signals from hundreds or thousands of pixels must be processed into a final output, signal compression is essential. However, this process can introduce signal loss due to overlap of each pixel. To mitigate this issue, logic circuits such as monostable circuits and ripple counters are commonly employed, which reduce the width of individual signals and intentionally introduce delays to minimize overlap. In this study, we have aimed to achieve reduced response time, prevent signal loss, and simplify the signal compression process through independent SPAD characterization and circuit design. The proposed SiPM is designed to export both energy and time information.

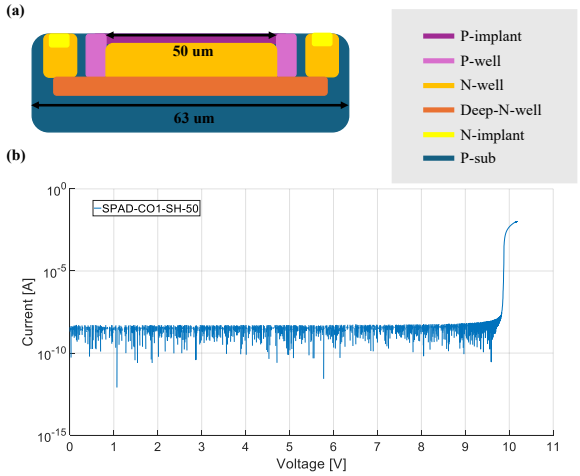

Fig. 2. (a) The cross-section of the SPAD, (b) the result of the I-V curve measurement.

2. Design of SiPM

Proposed SiPM was designed in common 180 nm CMOS process and the size of the chip is about 7.5 mm^2. A single pixel, including the SPAD and front-end, is arranged in a 20 × 20 array. Energy information is exported through 20 PADs, while the compressed signal is converted into timing information via a TDC. The control clock for outputting the energy information of each pixel is externally supplied to 20 rows.

2.1 Single Photon Avalanche Diode (SPAD) in Pixel

The SPAD used in each pixel was designed using the same fabrication process and underwent characterization, including I-V measurements, dark count rate (DCR) analysis, and light emission testing (LET). As shown in Figure 2, the SPAD was designed with a p+/n-well junction and incorporated a p-well guard ring. The measured breakdown voltage of the SPAD was approximately 9.8 V, with an active area of 50 μm and a total size of 63 μm.

In this study, the SPAD is controlled by a reset transistor, which functions as an active quenching circuit (AQC). The reset transistor operates based on a feedback structure [3]. Additionally, when an avalanche event occurs in the SPAD, it is immediately quenched by a 100 kΩ passive quenching resistor (PQR) in conjunction with the detector capacitance compensation (DCC).

2.2 *Single Pixel*

In the pixel, the comparator converts the photon signal into a digital signal as an externally applied reference voltage as shown as fig. 3 (a). Additionally, the comparator output is delayed through a delay cell and controls the reset transistor via a feedback structure, quickly turning the SPAD as 'off' state, reducing dead time, and increasing photon efficiency. Exported digital

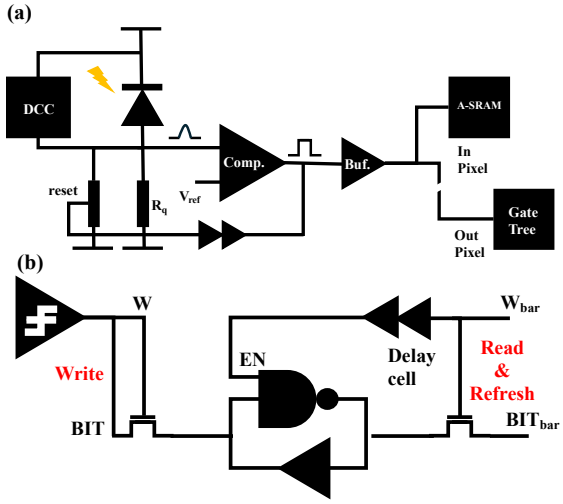

Fig. 3. (a) The schematic of single pixel, (b)The schematic of A-SRAM.

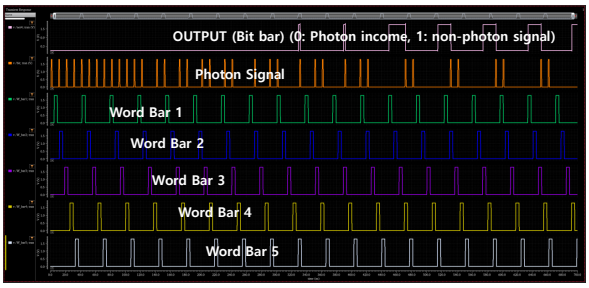

Fig. 4. Graph at the top shows the final output from five pixels. The first graph represents a triggered photon signal at 0, and the second graph is an arbitrarily simulated photon signal for function simulation. The five graphs below represent the signals entering each pixel.

pulse is connected to A-SRAM and gate tree as energy and time information.

2.2.1 Active-Static Random Access Memory (A-SRAM)

The active-static random-access memory (A-SRAM) is designed to export the signal as energy information in each pixels as shown in fig. 3 (b). When a photon signal is generated, it is converted into a digital signal through a comparator and then fed into A-SRAM via a buffer. Transformed signal is stored in a specially designed latch-up circuit through the transistor and is exported through BIT_{bar} when the external W_{bar} signal is applied as illuminated in Fig 4. Simultaneously, the W_{bar} signal, which is also externally applied from the other side, is delayed by 1 ns through a delay cell. After the signal is exported, the latch-up circuit is refreshed, resetting it to a state where it can receive the next photon signal.

To enable active refreshing of the A-SRAM, it is designed using the gate instead of the inverter, allowing signal acquisition while minimizing photon loss during additional compression processes. Moreover, the photon count frequency depends on the externally applied W_{bar} signal, and simulation results show a

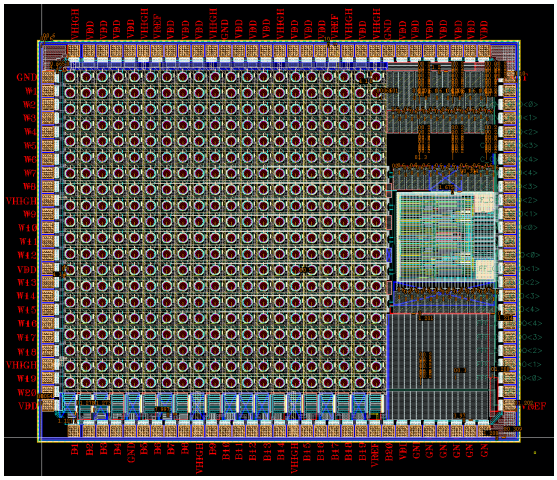

Fig. 4. The layout of the proposed d-SiPM.

maximum sampling rate of 1.5 GHz. However, in the designed A-SRAM, additional photon signals cannot be stored during the 'Read' state when the W_{bar} signal is applied, resulting in dead time. To reduce this issue, the durations of the 'Read' and 'Refresh' states in the A-SRAM must be minimized. This problem can be mitigated by applying a sufficiently fast W_{bar} signal of 1 GHz.

2.3 Wire Networking

Designed pixel The designed pixel array is configured in a 20 × 20 arrangement, with 20 BIT_{bar} lines routed externally. The signal for time information is initially compressed in the gate tree and then input into the TDC as a single signal. During the compression process, signal loss due to overlap may occur. Considering that the photon trigger probability in a typical SiPM follows a probability distribution centered around the middle, this study simplified the design to 100 pixels in the central region to mitigate this issue. As a result, a 3 mm × 2.5 mm d-SiPM was designed, as shown in Figure 5, with a total of seven metal wire layers in a mesh structure to facilitate signal transmission and reception between pixels.

3. Conclusions

In this study, the proposed d-SiPM was designed to achieve a high sampling rate while minimizing photon signal loss. Each pixel is equipped with a DCC and AQC to facilitate fast SPAD quenching, and a feedback structure was implemented to enable autonomous reset within each cell. Additionally, the signals generated by each pixel are temporarily stored in A-SRAM for a short duration before being output under the control of an external clock. Since the operating speed of A-SRAM is faster than that of the SPAD, signal loss that may occur during additional compression processes can be minimized. Furthermore, to optimize time information processing, the number of signals input to the TDC was reduced, thereby decreasing signal density while enhancing efficiency. The proposed d-SiPM has been successfully fabricated, and detailed design specifications and measurement results will be presented at the conference.

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