Radiation-Hardened ADC Design Using TMR Architecture

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1. Introduction

In radiation-rich environments, such as space, nuclear facilities, and high-energy physics applications, electronic circuits are vulnerable to radiation-induced failures. These include Single Event Effects (SEEs) and Total Ionizing Dose (TID) degradation. Such effects can result in functional disruptions, data corruption, or even permanent damage to semiconductor devices. Radiation-hardened by Design (RHBD) techniques have been widely adopted to ensure the reliable operation of analog and mixed-signal circuits in such conditions.

Among various analog components, Analog-to-Digital Converters (ADCs) play a critical role in signal processing systems by converting analog signals into digital data. There are several types of ADCs, including fully differential SAR ADC [1]. However, due to their sensitivity to radiation-induced transients, ADCs require specialized design methodologies to maintain accuracy and robustness under radiation exposure. One of the most effective RHBD techniques is Triple Modular Redundancy (TMR), which enhances system reliability by replicating critical circuit components and implementing majority voting logic to mitigate errors caused by radiation strikes. Several studies have used split-ADC architecture [2]

This paper explores designing and implementing an RHBD ADC employing TMR architecture to improve radiation tolerance. The proposed approach incorporates key circuit-level redundancy to reduce the error rate. We discuss the challenges associated with radiation effects on ADCs, the design considerations for integrating TMR, and the impact of RHBD techniques on system performance. Simulation results demonstrate the effectiveness of the proposed methodology in achieving high reliability in radiation-intensive environments.

2. Design Methodology and Circuit Implementation

We designed the proposed RHBD ADC using the Cadence Virtuoso EDA tool. The circuit architecture was implemented with TMR to enhance fault tolerance against radiation-induced single-event upsets (SEUs). The design process focused on optimizing the layout and conducting simulations at the transistor level to ensure the robustness of the ADC in environments exposed to radiation. A double exponential simulation was performed to assess the performance of the RHBD ADC. This simulation method effectively captures the impact of single-event transients (SETs) and enables a detailed analysis of the circuit's reliability.

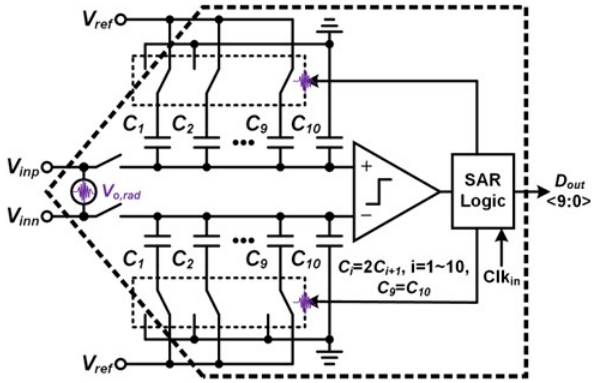

Fig. 1. Conventional fully differential SAR ADC

2.1 SAR ADC

Fig. 1 illustrates the fully differential Successive Approximation Register (SAR) ADC structure that uses a binary search algorithm to approximate the input voltage iteratively. It consists of a Track/Hold circuit to sample the input, a Comparator to compare it with the DAC output, SAR logic to control the approximation, and a DAC for conversion. The process continues until all bits are determined, producing an accurate digital output.

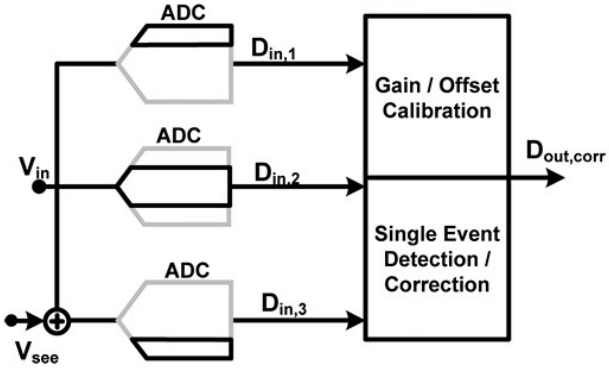

Fig. 2. Conventional split-ADC concept

2.2 Triple Modular Redundancy in ADC

Triple Modular Redundancy (TMR) is a fault-tolerant design technique that enhances system reliability by replicating critical components three times and using a majority voting system to determine the correct output.

If one of the three modules fails due to a radiation-induced error, the other two ensure the correct result is still produced. TMR is applied to protect against SEUs in radiation-rich environments.

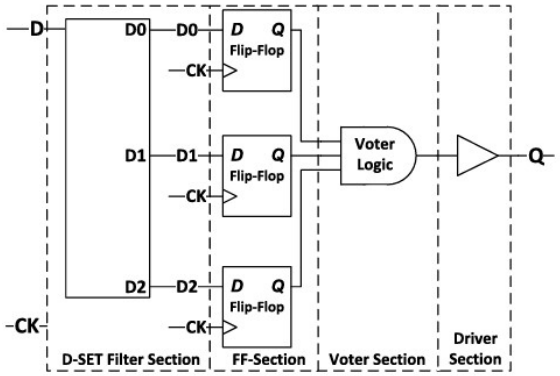

Fig. 3. Logical sections of the TMR concept [3]

2.3 Practical Application on Radiation Measurement

The proposed analog-to-digital converter (ADC) is specifically designed for applications in radiation measurement, delivering precise and reliable analog-to-digital conversion in radiation-rich environments. Its key features include a high resolution ranging from 10-bit to 12-bit for accurate signal acquisition, a sampling rate of 120 MS/s or higher, and a wide input voltage range of 0 to 3.3V, ensuring compatibility with a variety of sensors. Additionally, it boasts a low power consumption of ≤ 100 mW.

Table I: Target Specifications of ADC

Parameter	Target specification	Unit
Resolution	10 ~ 12	bits
Sampling Rate	≥120	MS/s
Input Signal Range	0 ~ 3.3	V
Signal-to-Noise-Ratio (SNR)	≥ 50	dB
Power Consumption	≤100	mW

3. Conclusions

In this paper, we presented the design and implementation of an RHBD ADC employing TMR architecture to enhance fault tolerance in radiation-prone environments. The SAR ADC architecture was selected for its efficiency, and TMR was integrated at critical circuit levels to mitigate single-event upset (SEUs). The design was implemented using Cadence Virtuoso, and its robustness was evaluated through Double Exponential simulations.

The proposed approach demonstrates improved reliability while maintaining performance efficiency. Future work will further optimize power consumption and explore additional radiation-hardening techniques to enhance overall circuit reliability.

Acknowledgements

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REFERENCES

[1] H. Jeon, I. Kwon, and M. Je, "Radiation-hardened sensor interface circuit for monitoring severe accidents in nuclear power plants," IEEE Transactions on Nuclear Science, vol. 67, no. 7, pp. 1738-1745, Jul. 2020

[2] H. Venkatram, J. Guerber, M. Gande, and U.-K. Moon, "Detection and correction methods for single event effects in analog to digital converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 12, pp. 3163-3172, Dec. 2013.

[3] O. Schrape, M. Andjelkovic, A. Breitenreiter, S. Zeidler, A. Balashov, and M. Krstic, "Design and evaluation of radiation-hardened standard cell flip-flops," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 11, pp. 4796-4808, Nov. 2021.