Field-effect transistor with electret layer for radiation sensor applications

Yongsu Lee^a, Jeong Min Park^a, Su Jin Kim^a, Han Soo Kim^a, Young Soo Kim^a, Jang Ho Ha^a, and Chang Goo Kang^{a*}

^aAdvanced Radiation Technology Institute, Korea Atomic Energy Research Institute

29 Geumgu-gil, Jeongeup-si, Jeolabuk-do, 56212 Republic of Korea

*Corresponding author: cgkang@kaeri.re.kr

1. Introduction

Recently, using polymer electret materials with semipermanent charge storage capabilities has emerged as a promising candidate in the field of non-volatile memory [1]. Polymer electret memory has the advantage of being capable of large-area solution processing at low temperatures, high compatibility with flexible substrates, and implementation with only a simple FET structure [2]. In this study, organic FET with a polymer electret layer for radiation sensor applications was demonstrated. This device can be manipulated with sufficient gate voltage and external light, and it causes non-volatile threshold voltage (V_{TH}) shifts. Furthermore, scaling is carried out by applying photo-lithography to organic FET. Therefore, it has a great possibility to be applied for a highly integrated programmable FET array, but also radiation sensor applications with proper scintillating layers.



Fig. 1. The fabrication process of DNTT FET with an electret layer. The process includes (a) buried gate formation, (b) Al₂O₃ dielectric deposition, (c) electret layer and DNTT channel deposition, (d) Au hardmask deposition and patterning, (e) electret/DNTT stack layers patterning, and (f) source/drain patterning. All patterning processes are proceeded with photo-lithography.

2. Methods and Results

2.1 Device fabrication process

Fig. 1 shows the Fabrication process of DNTT FET with an electret layer. First of all, a buried gate is formed on a Si/SiO₂ wafer (Fig. 1(a)). The buried gate enhances the electrical field uniformity on electret and channel layers [3]. Then, an Al₂O₃ gate dielectric is deposited using the atomic layer deposition process (Fig. 1(b)). On the insulating layer, 20 nm of poly(α -

methylstyrene) (P α MS) electret layer is formed using the sol-gel method, and then 50 nm of Dinaphtho[2,3b:2',3'-f]thieno[3,2-b]thiophene (DNTT) p-type organic channel is deposited using thermal evaporation process (Fig. 1(c)). To reduce the damage of the DNTT channel during patterning and etching processes, 30 nm of Au hardmask is covered on the DNTT channel, and patterned using photo-lithography (Fig. 1(d)). Therefore, electret and DNTT layers are protected, and uncovered regions are etched by O₂ plasma (Fig. 1(e)). Lastly, the device fabrication process is finished with the Au source/drain electrode patterning step (Fig. 1(f)).



Fig. 2. Demonstration of DNTT FETs with an electret layer. (a) is an optic image of the single FET with W/L = $16 \mu m/12 \mu m$ and (b) is an optic image of a chip containing 432 FETs. (c) is an electrical transfer curve of the DNTT FET, where $V_D = -2$ V.

2.2 Characteristics of demonstrated DNTT FET device

Fig. 2 shows the demonstrated DNTT FET with the P α MS layer. Using photo-lithography, a micro-sized organic FET device is successfully fabricated (Fig. 2(a)). As a result, this DNTT FET can be highly integrated with a CMOS-comparable patterning process, in which 432 devices are demonstrated on a 1.2×1.2 cm² Si/SiO₂ wafer (Fig. 2(b)). Fig. 2(c) shows a transfer curve of DNTT FET. It shows a typical p-type semiconductor characteristic with high electrical performances, so the fabrication process with photo-lithography seems to be well applied.



Fig. 3. Band diagram of DNTT FET with an electret (PaMS)

layer when (a) $V_{\rm G} < 0$ V and (b) $V_{\rm G} > 0$ V with light. The electret layer can store hole and electron charges.

2.3 Operation of electret layer on the FET

Fig. 3 shows the band diagram of DNTT FET with the electret layer. When negative $V_{\rm G}$ is biased, a hole charge on the DNTT channel is trapped at the P α MS layer, which causes a negative $V_{\rm TH}$ shift (Fig. 3(a)). On the other hand, when positive $V_{\rm G}$ is biased with sufficient light, a photo-induced electron is moved and trapped on the P α MS layer, causing a positive $V_{\rm TH}$ shift (Fig. 3(b)). Note that sufficient light condition is needed because of the lack of a minority carrier of DNTT.

3. Conclusions

The highly integrated organic FET with an electret layer was demonstrated. With semi-permanent charge storage properties of P α MS, this device has a stable and wide V_{TH} control range. Also, the external light operation makes it possible to apply the radiation sensing applications with proper scintillating layers such as CZT and CPB.

ACKNOWLEDGMENTS

This work was supported by the Korea Atomic Energy Research Institute (KAERI) Institutional Program (Project No. 523160-24 and 523510-24). This work was also supported by Grant RS-2022-00144108 funded by the Ministry of Trade, Industry and Energy of the Korean government.

REFERENCES

[1] Baeg, Kang-Jun, et al., Polarity effects of polymer gate electrets on non-volatile organic field-effect transistor memory, Advanced Functional Materials 18.22, pp. 3678-3685, 2008.

[2] Ling, Haifeng, et al., Effect of thickness of polymer electret on charge trapping properties of pentacene-based nonvolatile field-effect transistor memory, Organic Electronics 43, pp. 222-228, 2017.

[3] Lee, Sang Kyung, et al, Advantages of a buried-gate structure for graphene field-effect transistor, Semiconductor Science and Technology 34.5, p. 055010, 2019.