High Speed Active Quenching for Single-Photon Avalanche Diodes Using Digital Radiation Detection

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1. Introduction

The single-photon avalanche diode (SPAD) detector is widely utilized across various applications such as LiDARs, time of flight (ToF) 3D imaging, and positron emission tomography (PET) scanning due to its exceptional sensitivity, pico-second timing resolution, low cost, and low power consumption [1]-[2]. A basic SPAD detector cell comprises an avalanche photodiode, a quenching and recharging circuit, and a readout circuitry. While passive quenching circuits are simple, they suffer from slow quenching and recharging, limiting the maximum photon-counting rate and increasing the afterpulsing probability (AP). To address these limitations, active quenching, which rapidly lowers the diode bias below breakdown to stop the avalanche, was introduced. Active quenching offers advantages such as higher maximum photon-counting rates, lower afterpulsing probability, and reduced jitter of photon arrival time, making it favorable for ToF applications. However, active quenching circuits may occupy a large area, reducing the fill factor of SPAD detector cells. Thus, it is crucial to implement an active quenching circuit as compact as possible while maintaining quenching performance. The proposed detector capacitance compensation (DCC) technique aims to enhance active quenching operation without significantly increasing power or area requirements compared to conventional designs. This paper will elaborate on the DCC technique and present simulation results of the proposed active quenching circuit.

2. Methods and Results

In this section, the modeling of SPAD, full architecture of proposed circuit, simulation result, and layout comparison to conventional design are described.

2.1 Detector Model

Basic electrical modeling of SPAD was used to provide an input signal for simulation, shown in Fig. 1 [3]. Breakdown voltage (V_{BD}) is measured to be 15 V. R_D and C_D values are tuned to mimic the output signal of SPAD according to the information given by previous taped-out chips. All the other design parameters are kept equal except for the DCC technique for a fair comparison. An ideal voltage source provides the high voltage to the CATHODE node through a ballast series resistor.

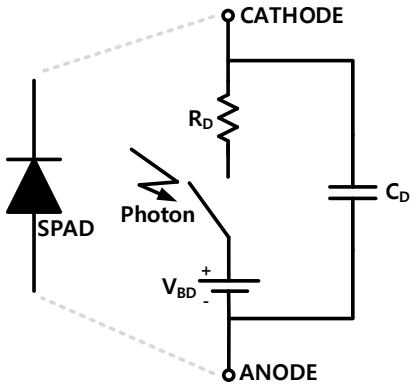

Fig. 1. Basic electrical modeling of SPAD for simulation.

2.2 Full Architecture

Fig. 2 shows the full circuit architecture of the proposed active quenching circuit. Cadence Virtuoso was used to implement and simulate the circuit. We employed the conventional active quenching circuit from [4] and then merged it with a DCC amplifier. The DCC amplifier is implemented as a source-follower structure using only two transistors. We reduced the number of transistors required to implement a DCC amplifier, introduced in [5]. V_{SPAD+}, V_{hold_off}, and RESET signals are biased outside the chip.

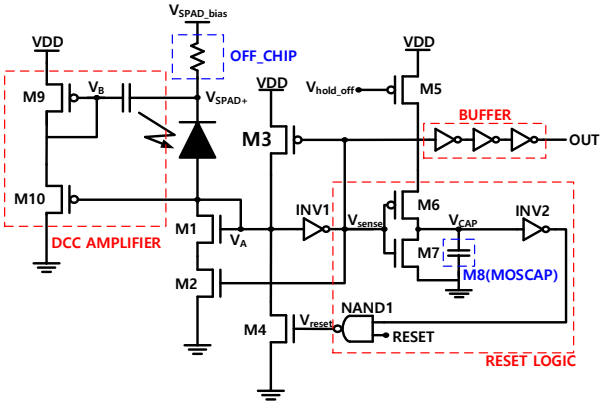

Fig. 2. Full architecture of the proposed circuit.

2.3 Simulation Result

The simulation result is shown in Fig. 3. The conventional active quenching circuit takes about 4.55 ns to reach half VDD, while the proposed active quenching circuit takes about 1.59 ns, which is almost three times faster. As explained above, the simulation result clearly shows that the DCC technique effectively boosts the quenching operation until the anode node reaches half VDD.

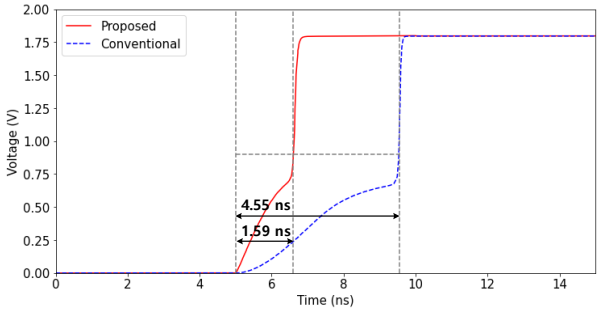

Fig. 3. Simulation results of active quenching at node V_A (Red solid: proposed, blue dashed: conventional).

2.4 Layout Comparison

The chip layout is shown in Fig. 4. The MIM capacitor is laid on the top of the active quenching circuit, yielding no additional area. Besides the SPAD, the circuit width increased by 4.4 μm for the implementation of a DCC amplifier. It is only about a 23 % area increase in total, which is acceptable considering about three times better quenching time.

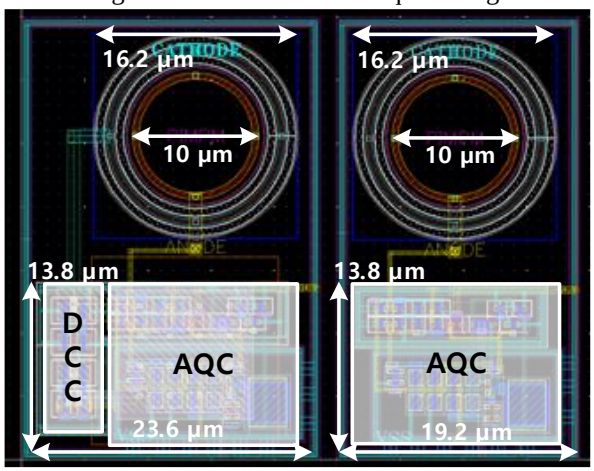

Fig. 4. Layout (Left: proposed, right: conventional).

3. Conclusion

SPAD requires fast quenching to achieve a higher photon counting rate and minimize jitter and afterpulsing probability while maintaining compact active quenching size and affordable power consumption. In this work, the DCC technique boosting double active quenching of SPAD with minimized area overhead and low power has been designed in a 0.18 μm CMOS technology. The simulation results confirm almost three times better quenching performance with an overhead of a mere 23 % area increase compared to the conventional design. When applied in fields where quenching performance is important, such as PET, the proposed circuit offers a favorable solution. The comparison is made between the conventional design and the proposed design by employing the same SPAD for every circuitry.

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