Implementation of an Image Display Unit for a Portable Gamma Camera

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1. Introduction

A gamma camera is a kind of imaging device that combines the position of radiation sources with an optical camera image and can be used to visually secure the position of the radiation source to ensure safety from radioactive materials [1]. It is also used in biomedical imaging device such as positron emission tomography (PET), or small-animal imaging systems [2, 3]. When manufactured as a portable type, the system complexity should be reduced. In this paper, a simple image display unit for a portable gamma camera using a field programmable gate array (FPGA) (10CL006) is proposed. Applying 10CL006 to a portable gamma camera system has an advantage. It can be implemented cost-effectively since the size of embedded memory and the number of multipliers is the minimum compared to other Cyclone 10 LP series processors [4].

2. System Implementation

2.1 Image Display Unit

The operating frequency of the complementary metal oxide semiconductor (CMOS) camera is 24 MHZ, and each pixel of data transmits a 16-bit color data signal to the FPGA. It processes 480x272 pixels of data per frame, and the data color signals of red, green, and blue (RGB) of each pixel are stored in a synchronous dynamic random-access memory (SDRAM). SDRAM is used to process image data from the CMOS camera to the LCD. The color data is stored in SDRAM using first-in, first-out (FIFO) memory since the SDRAM operates at 100 MHz, which is faster than the CMOS camera's operating frequency of 24 MHz, and each module operates asynchronously. The operating frequency of the liquid crystal display (LCD) is 9 MHz. Also, the image data is displayed on the LCD using FIFO memory. It is programmed in Verilog, and FIFO memory and phase-locked loop (PLL) are used through Quartus FPGA Intellectual Property (IP).

2.2 ADCs for Anger Logic

The silicon photomultiplier (SiPM) detects gamma rays, and it typically has four channel outputs [5, 6]. After the ADC samples pulse signals from those outputs, the position of the gamma-ray source can be determined by Anger logic. ADCs can sample up to 125 MHz and have a resolution of 12 bits. The trigger signal is generated when all four channels exceed a certain level of voltage. The position is displayed on the LCD in a yellow square according to the Anger logic.

2.3 Resource Usage of the FPGA

The input and output (I/O) pins of the FGPA can include those of a COMS camera, SDRAM, LCD, and four-channel ADCs. I/O pin usage is 72%, logic element usage is 73%, embedded multiplier usage is 77%, and internal memory usage is 5%. Table I and Figure 1 show the design specification and block diagram of the image display unit, and Figure 2 shows the implemented unit.

3. Conclusions

An image display unit for a portable gamma camera is proposed using 10CL006. It is eligible as a signal processor for portable gamma cameras since it provides enough resources for image signal processing, and its complexity and cost are relatively low. A Verilog-based program is used to process pulse signals generated from SiPM. After estimating the position of the radioactive source from the pulse signal of a SiPM array using Anger logic, it displays the location of the source on the camera image.

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Table I: Design Specification

FGPA	CMOS Camera	SDRAM	LCD	ADC
Intel 10CL006	OV5640 (24MHz)	256Mb (100MHz)	480 x 272 (9MHz)	12bit x 4 Ch. (upto 125MSPS)

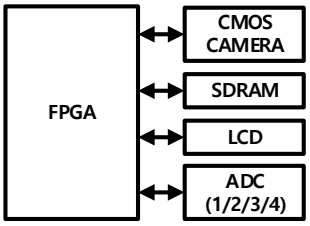

Fig. 1. Block diagram of the image display unit.

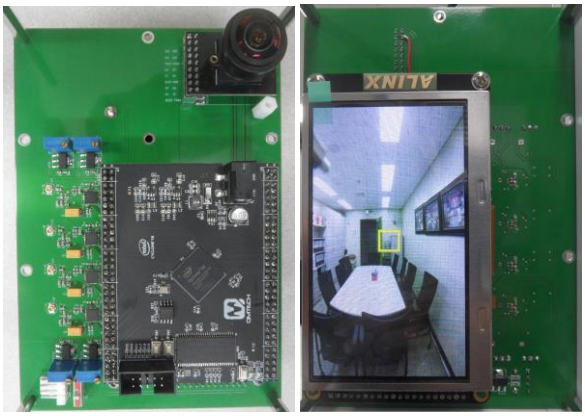

Fig. 2. Implemented the image display unit (front and back).