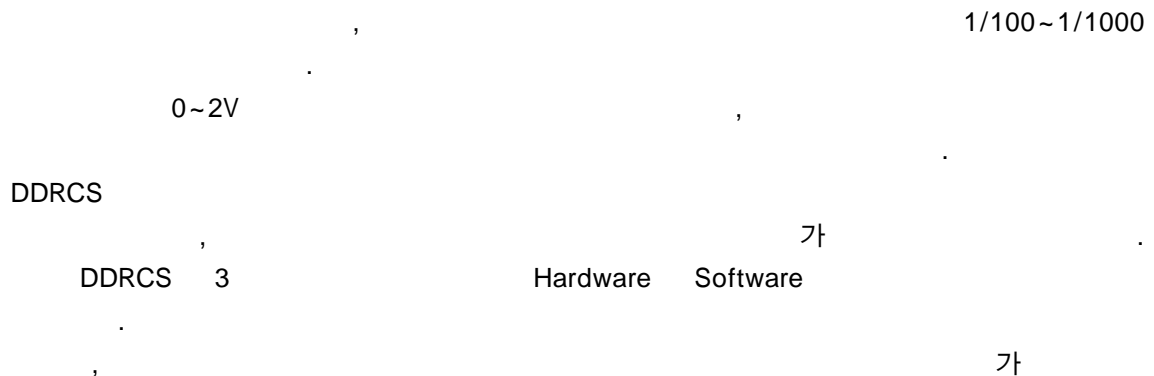


동적 제어봉 제어능 측정 장치 개발

Development of Direct Digital Reactivity Computer System (DDRCS)
for Dynamic Control rod Reactivity Measurement(DCRM)

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Abstract

Neutron Flux level may be rapidly decreased to 1/100~1/1000th order of magnitude during DCRM(Dynamic Control rod Reactivity Measurement) test. Because the conventional DRCS(Digital Reactivity Computer System) converts NIS current signal to analog one with the range from 0 to 2 volt, and computes reactivity, the DRCS can not measure the widely changed flux level during DCRM test. The DDRCS(Direct Digital Reactivity Computer System) which is developed in this study can measure the current of all the range directly and reduce the burden to maintain the equipments, because of its simplified structure. The function of DDRCS was fully validated through three times of plant low power physics tests. The software program to handle all the items of low power physics test will be developed.

1.

가

()

(Rod Swap Method)

12

(Dynamic Control rod Reactivity

Measurement Method, DCRM™)

가

2

가

가

Direct Digital Reactivity Computer System(DDRCS)

2.

(NIS)

(100 nAmp ~ 1 nAmp) In-hour

/

가

가

가

Westinghouse

ABB-CE

Analog

가 KINS가

Digital

Digital Reactivity

Computer

(Electrometer)

(, ,)

(0

2V)

1 2

/

/

/

(, ,)

가 / 가 . 가
가

(1)

200nA, 20nA, 2nA) [1] (2 μ A, 가

(2)

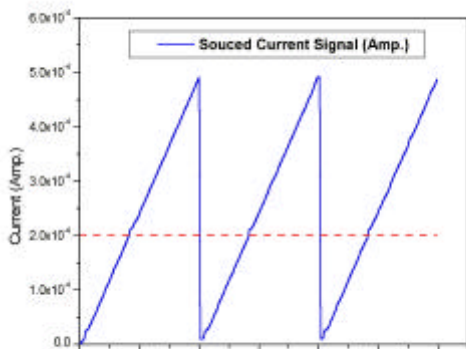
2nA , [2]

(3)

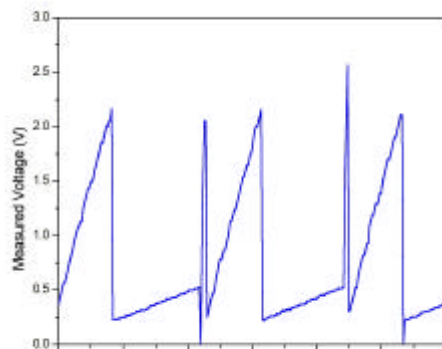
, A/D [3]

(4)

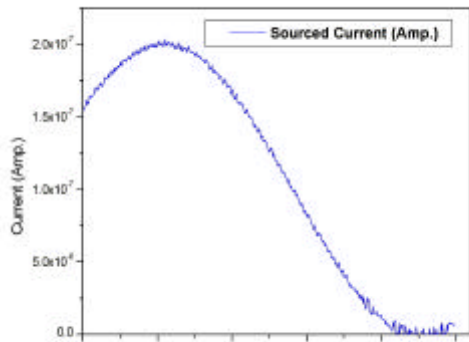
3 가 / (,) A/D [4]
가 Auto Range Mode
3 4 (0 0.17V. 1.73
2.0V) 가



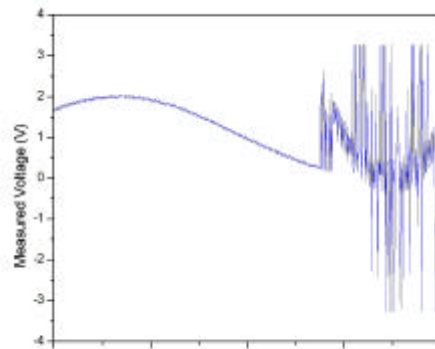
[1]



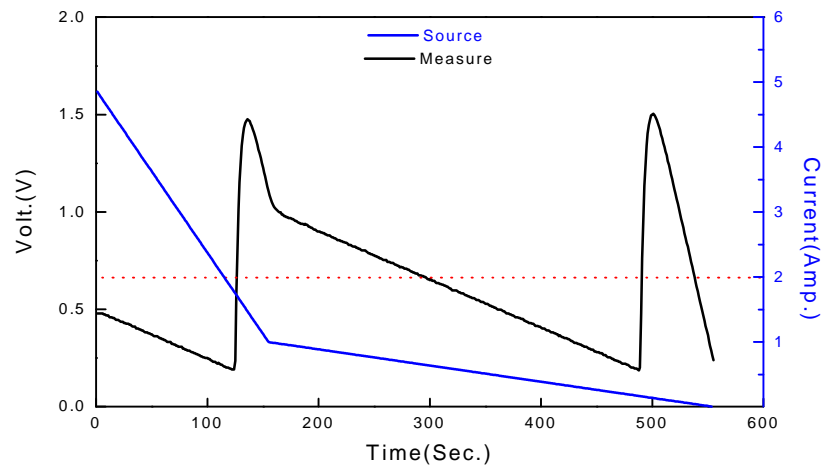
1



[2]

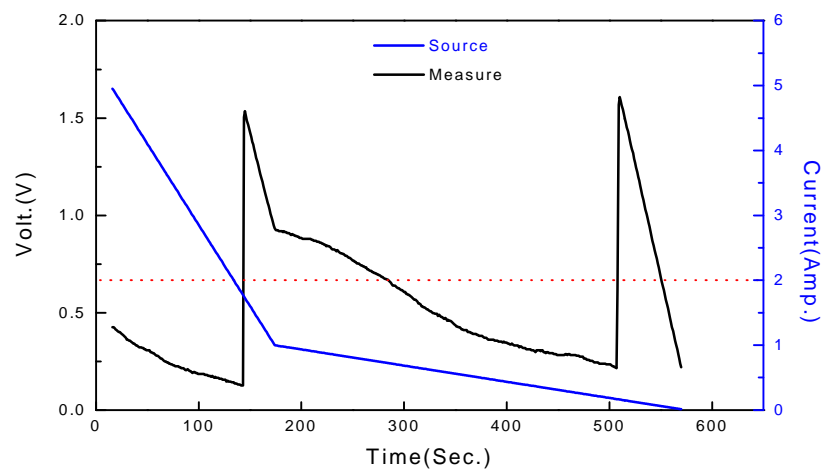


2



[3]

3



[4]

4

3. DDRCS

DDRCS(Direct Digital Reactivity Computer System) , . DDRCS 가

. [5] DDRCS PC 가 ,

PC Keithley Model 2400 Digital Source Meter . 가
1nA 1pA 가

Keithley Model 6514 Electrometer Model 428 Current Amplifier . Model 428
Range 가 , Model 6514 가 , 2

가 . Model 428 Embedding

DDRCS (Adwin-pro) A/D

16 , 0.01ms . 가
Clock 40MHz 250ns 가

PC Recorder micro second .
USB Ethernet , Chart

가 .
Chart Recorder .
PC , 가

Model 6514 PC .
DDRCS가

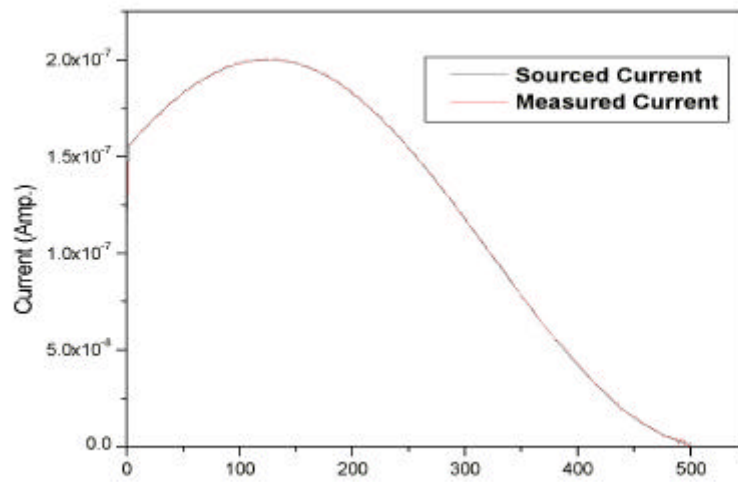
(1) (sine)

[6] 가

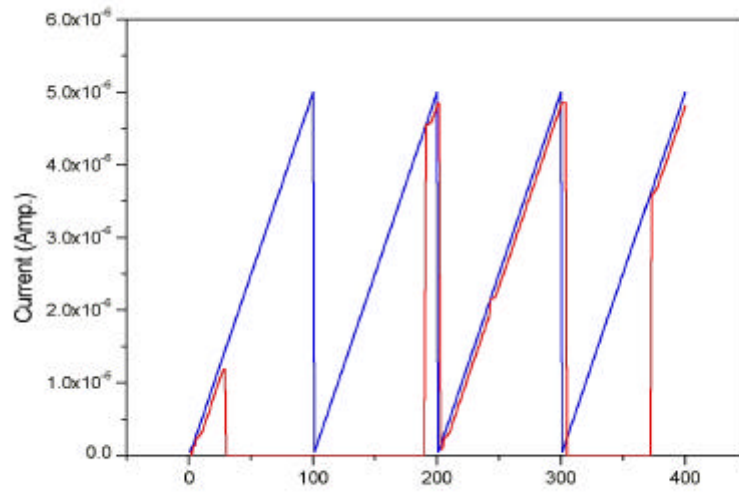
(2) 2 13 , /



[5]



[6] DDRCS 1



[7] DDRCS 2

4.

2001 10 13 2 13 3 D,B

/ DDRCS [8] 2 13

Background

DDRCS 가 30 D, B

. D D D, B Background

2002 3 7 1 14 D,C,B,A ARO 40 60pcm

D 183step
D ARO

Background

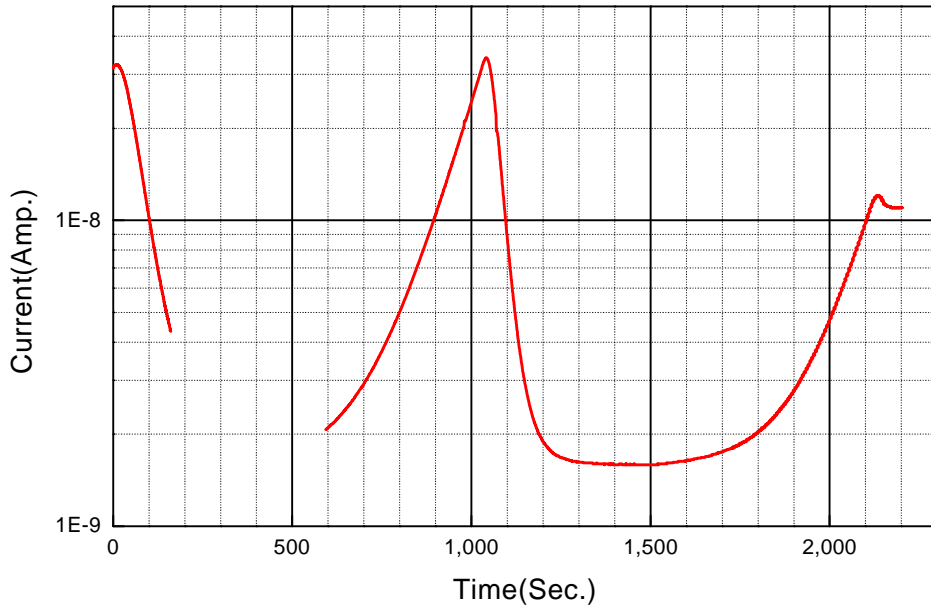
D D,C,B,A / D
48step

가 , ARO

70%

6step

6step



[8] 2 13 DCRM

10

[9]
1 20

[1]

/

3 7

, CE

2002 4 13 20

30

5, 4, 3,

B7

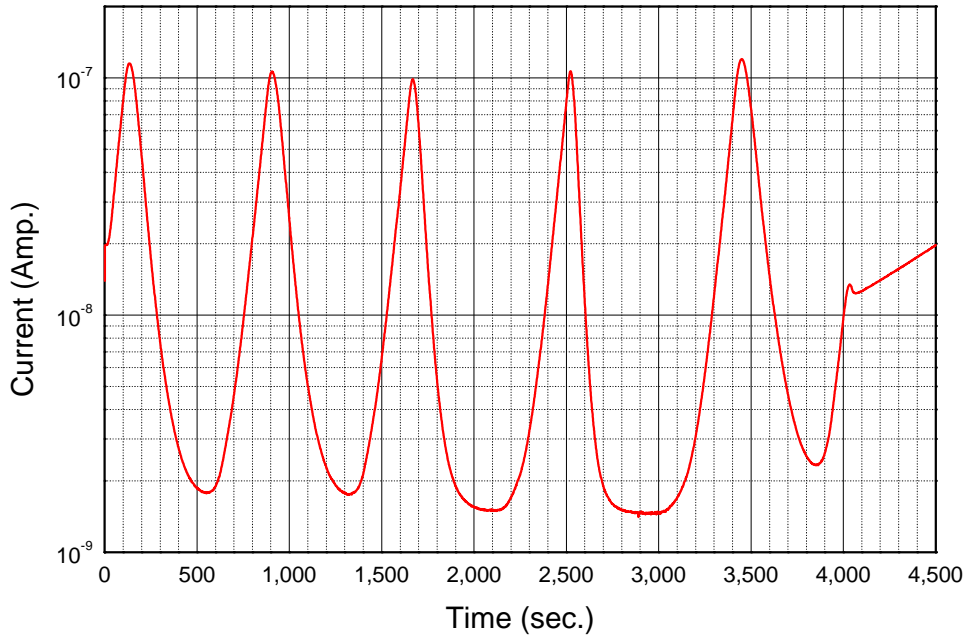
가 1
가 4

20pcm 가
1

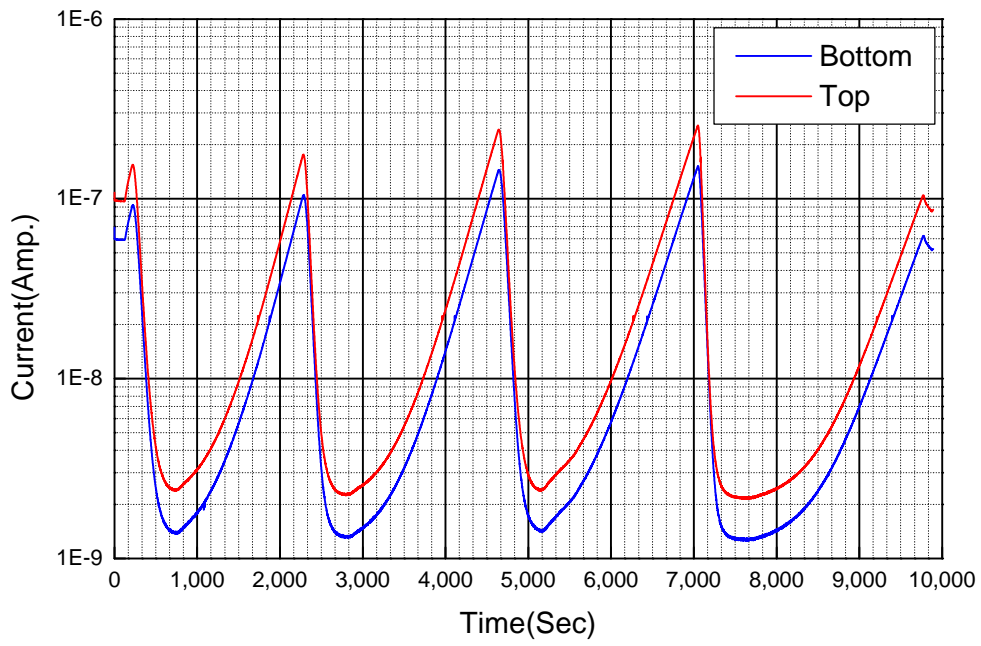
1

[10]

2 50



[9] 1 14 DCRM



[10] 3 7 DCRM

| | | | (Stop watch Time) |
|---|-----------------------------|----------|-------------------|
| | | 10:50:39 | 00:00:00 |
| D | D (183step - -> 225step) | 10:50:54 | 00:00:15 |
| | D (225step) | 10:51:47 | 00:01:08 |
| | D (225step - 6step) | 10:52:15 | 00:01:36 |
| | D (6step / - 225step) | 10:56:51 | 00:06:12 |
| | D (225step) | 11:01:31 | 00:10:52 |
| | D (225step - 6step) | 11:05:07 | 00:14:28 |
| | D (6step / - 225step) | 11:09:43 | 00:19:04 |
| | D (225step) | 11:14:23 | 00:23:44 |
| C | C (225step - 6step) | 11:17:55 | 00:27:16 |
| | C (6step / - 225step) | 11:22:37 | 00:31:58 |
| | C (225step) | 11:27:17 | 00:36:38 |
| B | B (225step - 6step) | 11:32:17 | 00:41:38 |
| | B (6step / - 225step) | 11:36:58 | 00:46:19 |
| | B (225step) | 11:41:38 | 00:50:59 |
| A | A (225step - 6step) | 11:47:17 | 00:56:38 |
| | A (6step / - 225step) | 11:51:59 | 01:01:20 |
| | A (225step) | 11:56:43 | 01:06:04 |
| D | D (225--> 183step) | 11:57:14 | 01:06:35 |
| | D (183step) | 11:58:06 | 01:07:27 |
| | | 12:06:17 | 01:15:38 |

5. DDRCS

DDRCS

/

3

가

DDRCS

가

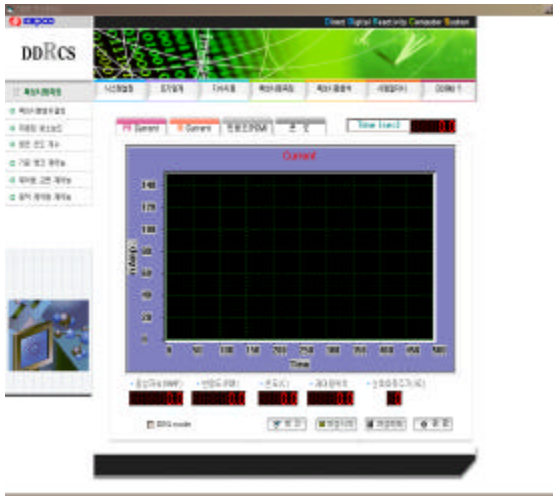
GUI . [11] DDRCS
 GUI 가 . [12]
 , [13]



[11] DDRCS GUI



[12]



[13]

6.

0~2V

1/100 ~ 1/1000

DDRCS

DDRCS 3

Hardware Software

, 가
가 .

7.

1. “ , ” , 1992
2. “가 (), ” ,
2001
3. , “ 1 14 , ” 2002