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A New CMOS Bandgap Reference Voltage Generator for CMOS APS Imager

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Abstract

For the proposed CMOS Bandgap Reference (BGR) generator reducing the circuit area to be imbedded in CMOS Active Pixel Sensor (APS) imager, the responses of temperature and radiation were tested. The design target of V_{DD} and V_{ref} for the BGR are over 2.5V and 0.75V with ±5% margin, respectively. The BGR hired level shift differential op-amp biased with cascode bias circuit in feedback loop in order to perform low-voltage operation and high output impedance characteristic. The BGR was implemented in a 0.18um triple well two-poly five-metal process using the Hynix 0.18μm CMOS process. Temperature variation and total ionization dose (TID) effect under Co-60 exposure conditions for the BGR were evaluated by each measurement of V_{ref}. In temperature response, the % changes in the V_{ref} were 0.128 and 0.768 for 45°C and 70°C, respectively from the V_{ref} at 25°. The measured V_{ref} changes for the radiation dose were 2.466% and 4.612% for 50krad and 100krad, respectively from the V_{ref} at 25°C and zero dose

I. Introduction

The bandgap reference (BGR) circuit is one of the most popular reference voltage generators that are hired in high precise comparators, A/D or D/A converters, and other analog circuit. The main role of BGR is to support a stable reference voltage and/or current to an integrated circuit and this stable reference should not be dependent of supply voltage fluctuation. The requirement of BGR, other than the stable of voltage and/or current, is insensitive to temperature variations.

Related to the BGR, several unique solutions had been suggested [1], [2], [3] and experiment results under sever condition such as radiation also had been performed [4]. Among other mixed signal circuit, CMOS image sensor, which is used in the field of X-ray imaging as well as general vision area, also needs the BGR in order to provide stable reference voltage.

In this paper, we present another circuit solution and test results of both temperature response and radiation response for the BGR, which will be imbedded in the CMOS APS

image sensor. The main focus of this paper is to evaluate the performance of the newly proposed BGR under the condition of temperature and radiation dose instead of explaining in detail the reason for both two responses of the BGR.

II. PROPOSED BGR CIRCUIT and ITS PERFORMANCE

The key idea of the proposed bandgap reference, shown in Fig1, is to use cascode current mirror with wide swing and especially, controlling the size ratio of PMOS transistors in the current mirror can lead to reduce the ratio of the emitter area of the PNP bipolar transistor, Q1:Q2 into 1:10, which can be less variation of V_{ref} for the V_{DD} changes. In the part shown in dotted line, the size ratio of PMOS transistors, 2Wp:Wp where 2Wp means two time of the width of the PMOS transistor makes two times of current flow. However, we use two PMOS with the same Wp/Lp since two times of PMOS width actually do not make two times of current flow in real.

The differential op-amp biased with cascode bias circuit is used in a feedback loop having the performance of low-voltage operation and high output impedance characteristic for the proposed BGR. The proposed BGR incorporates two types of bias circuits; one generates the current that is proportional to VBE and the other generates the current which is proportional to V_T. This two-type bias method makes it possible to reduce the number of diodes.

In this circuit, level shifter is located before input part of the differential op-amp, which elevates the input bias voltage of the differential op-amp and this causes all transistors in the differential op-amp to be operated in the saturation region. Using the level shifter is to have opportunity to be manufactured in the process providing only normal thermal voltage V_T without low- V_T MOS transistor.

If we use simple current mirror instead of the cascode current mirror in the BGR, the current value in the current mirror may be changed by channel length modulation and this also makes the value of the V_{ref} fluctuation in case that the target voltage of the V_{ref} is not equal to the V_{BE}.

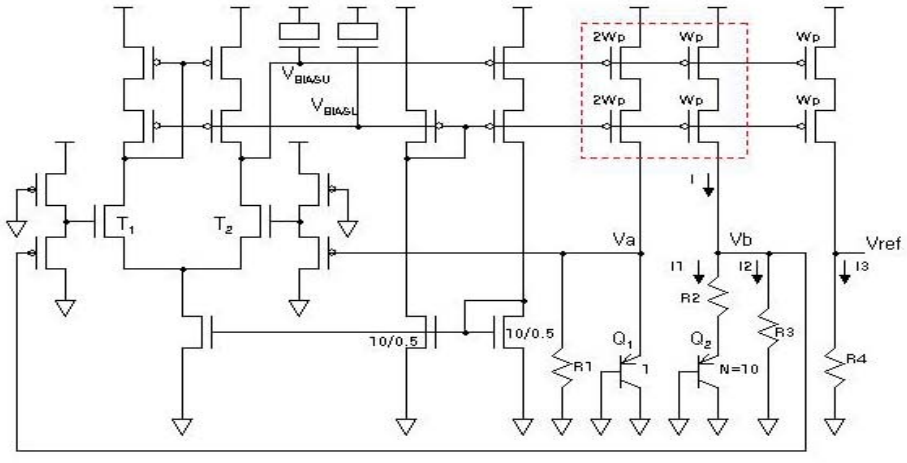

Fig. 1. Proposed Bandgap Reference Circuit

In the circuit of Fig. 1, the resistances of R1 and R3 are equal, and the voltages of V_a and V_b are controlled to be the same by adjustment of the level shifter and the differential op-amp. The current I is $I_1 + I_2$, and I_1 and I_2 is proportional to ΔV_{BE} and V_{BE1}, respectively since as following relations.

$$I_1 = \frac{\Delta V_{BE}}{R_2}, \qquad I_2 = \frac{V_{BE\,1}}{R_3} \tag{1}$$

where ΔV_{BE} is the forward voltage difference between the two BJT Q_1 and Q_2,

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_T \ln(kN) \tag{2}$$

In equation (2), V_T, k, N are the thermal voltage, the number of PMOS transistor, and the area of BJT emitter.

Here, I is mirrored to I3 and therefore, the output voltage of the proposed BGR, $V_{ref,}$ becomes

$$V_{ref} = IR_4 = (\frac{V_{BE1}}{R_3} + \frac{V_T \ln(k\,N)}{R_2})R_4 \tag{3}$$

By choosing the appropriate resistance ratio and the fixed values of k=2 and N=10, the V_{ref} will be lower than the silicon bandgap which means it is insensitive to temperature dependence [5] as other proposed BGR. As in the general cases of a bandgap reference, the proposed BGR also shows that the output voltage of the BGR is the sum of a forward voltage difference between two BJT Q_1 and Q_2 and a voltage that is proportional to absolute temperature (PTAT).

Fig. 2 shows a start-up circuit for the BGR. The V_{ref} does not act normally if V_{BIASU} and V_{BIASL} follow the V_{DD} voltage by coupling the capacitor at power-up because the bias current becomes zero.

If the V_{BIASU} of Fig. 2 is larger than the (V_{DD} − |V_{TP}|), the PMOS transistor, MP1, becomes OFF and because the NMOS transistor, MN1, becomes ON as N1 rises by the V_{DD}, the V_{BIASU} voltage is discharged. The V_{BIASL} acts similarly and the V_{BIASU} and the V_{BIASL} of BGR make bias operation normally. Here, the V_{TP} is the threshold voltage of the PMOS and the N1 is the gate node of the MN1 transistor.

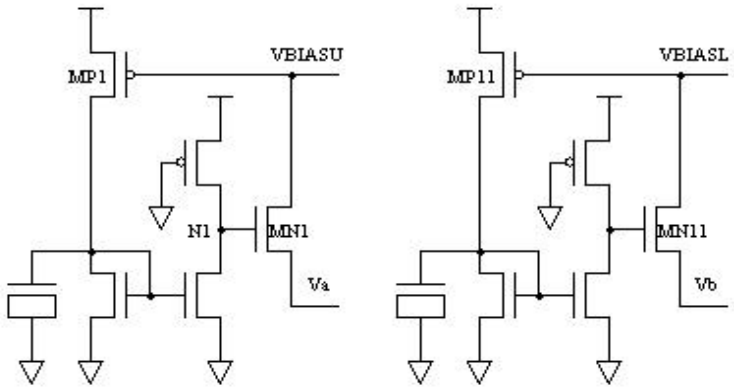

Fig. 2. Start-up circuit of the proposed BGR circuit

With the proposed BGR including the start-up circuit, we estimated the performance of the temperature response by SPICE simulation tools using the Hynix 0.18μm CMOS process parameter. The design target of the V_{DD} and the V_{ref} are over 2.5V and 0.75V having ±0.5mV margin, respectively. Figure 3 shows the results of simulation for the response of temperature.

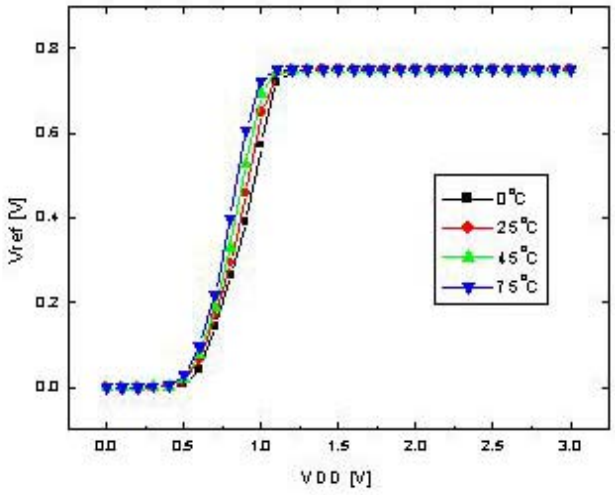

Fig. 3. Simulation results of V_{ref} for the BGR with temperature variations

The % changes in the Vref from the value of 0.751 at 25°C were 0.04242, -0.00325, -0.05386 for 0°C, 45°C, and 70°C, respectively. These simulated results well satisfied the purpose of the proposed BGR.

III. Experiment Results And Discussion

A. Test Chips

The proposed BGR was implemented in a 0.18um triple well two-poly five-metal process using the Hynix 0.18μ m triple-well CMOS logic process that have normal V_T transistor. Figure 6 shows the photograph of the proposed BGR test chip from the Hynix 0.18 μ m process. After testing with memory testing equipment, the minimum operation voltage was 1.2V, temperature fluxion was 207ppm/° C, and operating current (between V_{DD} and V_{SS}) was sub-10μ A. The measured distributions of the V_{ref} shown in Fig. 5 over 120 samples had the average V_{ref} of 759mV with σ=25.4 mV.

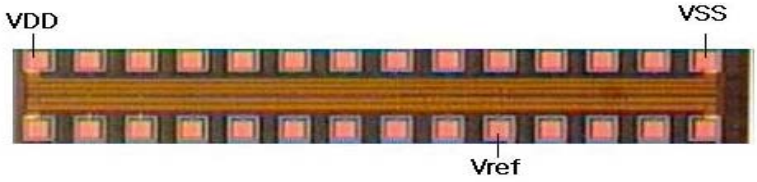

Fig. 4. Test chip microphotograph of the proposed BGR on wafer and their test points

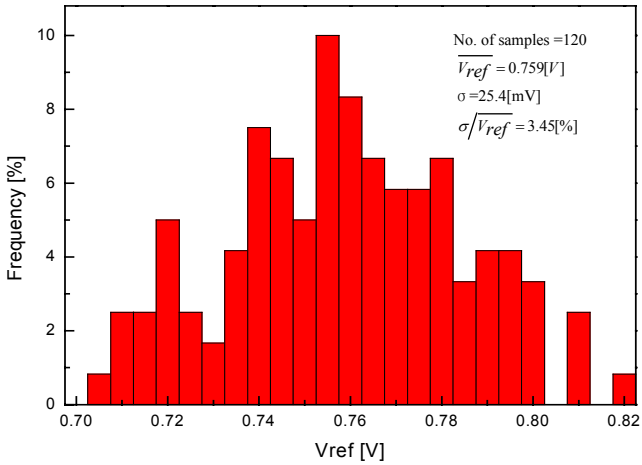

Fig. 5. Measured distributions of V_{ref} for 120 samples at V_{DD} (2.5V) and temperature (25°C)

B. Temperature Response of the BGR

In order to see the temperature variations of the BGR, we selected one of the samples that has the V_{ref} of 0.781 at 25°C. The changed values of the V_{ref} from the value of 0.781 at 25°C were 0.782 for 45°C and 0.787 for 70°C, and the % changes in the V_{ref} were 0.128 and 0.768, respectively from the V_{ref} at 25°C.

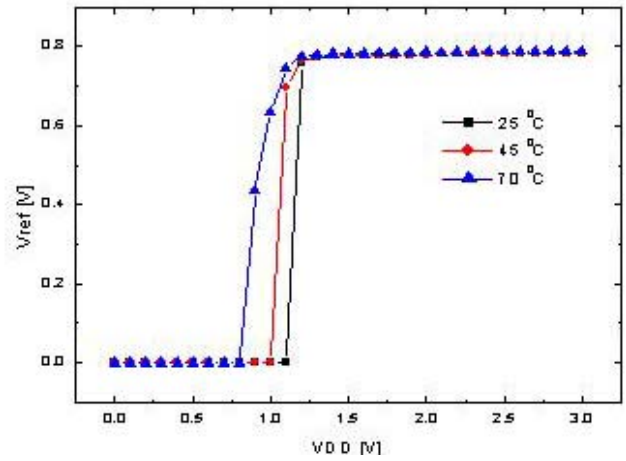

Fig. 6. Measured V_{ref} with changing V_{DD} for different temperatures (25°C, 45°C, 70°C)

Through the equation (3) we expected that the V_{ref} of the proposed BGR is little dependent on the temperature by determining appropriate resistance ratio of R2, R3, and R4. Changing R4 value may get the desired reference voltage. This BGR, therefore, basically follows the conventional with almost the same performance of temperature response but has an additional advantage of reducing the size of BJT emitter, N=10, which finally minimize chip area compared to others [1], [2].

C. Radiation Response of the BGR

The radiation response test, total ionization dose (TID) effect of the V_{ref} change, for the BGR was performed using Co-60 gamma source in KAERI experiment setup. The source to wafer distance was 16cm and dose rate was 5krad/hr. The V_{ref} measurements were performed using HP4155A- semiconductor parameter analyzer in the probe station.

The radiation response of the BGR for the increasing dose rate was shown in Fig. 7 and Fig. 8.

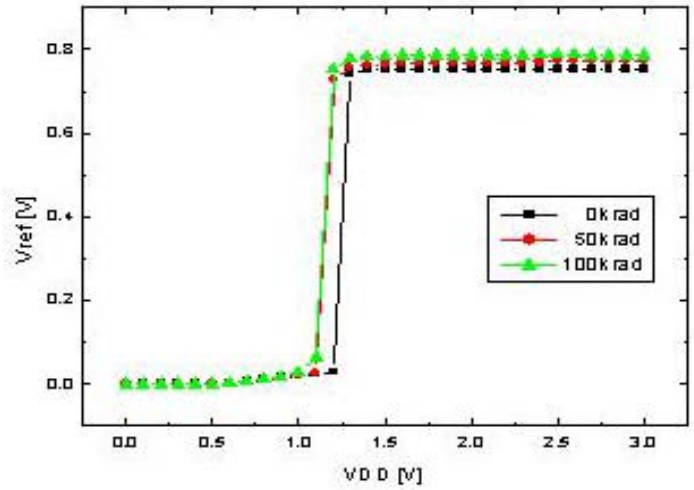

Fig. 7. Measured V_{ref} with changing V_{DD} for radiation doses from 0krad to 100krad at room temperature

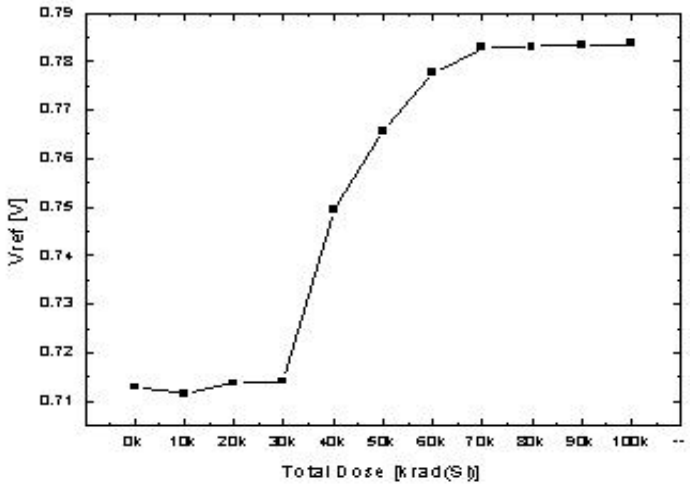

Fig. 8. Measured V_{ref} at V_{DD} of 2.5V for radiation doses from 0krad to 100krad

The left shift of the V_{DD} in Fig. 7 and the remarkable change of the V_{ref} in Fig. 8 were appeared. Especially, the fluctuation of the V_{ref} up to 40krad, a steep increase of the V_{ref} from 50krad, and no more increase of the V_{ref} from 70krad were found in the measured results. The V_{ref} for one of the selected samples at room temperature and zero dose was 0.752 at the V_{DD} of 2.5. The changed values of the V_{ref} of the sample were 0.779 and 0.784 for 50krad

and 70krad, and those were the change of 2.466% and 4.535% in the V_{ref}, respectively. Especially, at 20krad for the BGR, the % change in the V_{ref} was 0.11, which is similar to REF02 model of ADI manufacture [4] with acceptable performance.

Compared to the results of the temperature response, the V_{ref} variations to the radiation response were relatively more severe but it is not expectable that the V_{ref} variations may be out of designed margin ±5% at over 100krad.

Basically, it is possible that the reasons for the radiation response of the BGR can be explained by TID effect since one of the cumulative effects in semiconductor devices for gamma irradiation is that one, which is generally due to the charge trapping in the oxide layer [6].

In MOS devices, the TID effects induce the degradation of mobility, the shift of threshold voltage, and the increase of leakage currents. As in the case of MOS devices, for the BJT the TID effects also induce the degradation of mobility and the increase of leakage currents, resulting in gain degradation. Therefore, the electrical characteristics of the devices may be the results of the combination of the internal structure and affected by the amount of the TID [7], [8], [9].

In the BGR, however, the combination of the changed electrical properties of the discrete devices makes more complicated to understand of the V_{ref} change by the radiation dose. For the TID effects in the BGR, it is expected that DC biasing point be shifted in MOS differential amp. In Fig. 1, there can be mismatch between two threshold voltages, V_{t1} and V_{t2}, for MOS transistors, T_1 and T_2, respectively if the DC bias point is changed by increasing the radiation dose, which is resulting in offset variation. This also influences on the precision of the cascode current mirror that should be operating at saturation mode. The mismatch of other electrical parameters such as conductivity, threshold voltage, and gain can also induce currents mismatch in the current mirror and finally change the V_{ref} by the radiation dose.

VI. CONCLUSION

In this paper we proposed the BGR for one of the methods to minimize chip area with acceptable performance by reducing the ratio of the emitter area of the PNP bipolar transistor, Q_1:Q_2 into 1:10 and can get free reference voltage by controlling the resistance in the circuit.

For two response results of both temperature and radiation, the proposed BGR can be less variation of V_{ref}.

Even though the variations of the V_{ref} in the radiation response were relatively larger than those in the temperature response, it can be also allowed to operate the BGR in the condition of insensitivity of the radiation dose since ±5% is general margin for Vref.

VII. REFERENCES

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