

# Bus Accessing Performance Evaluation for Plant Control System

Yangmook Chung

Korea Hydro and Nuclear Power Co., Ltd.#84-1, Bugu-ri, Buk-Myeon, Ulchin-gun, Kyong-buk Korea  
Tel: (054)785-2347, Fax: 2369, Email: jungyam@khnp.co.kr

## 1. Introduction

The PCS system with 44 communication masters(CM) which process more than 30000 input and output signals, designed and manufactured by HF Contorols Corporation, is applied to UCN #5,6 nuclear power plant for the first time. In the process of system operation, the numerous problems have been issued and investigated and fixed so far. To share a understanding for digital communication system, UCN PCS communication methods are described herein through comparisons between the different priority techniques as well as the results of performance tests.

## 2. Bus Arbitration Schemes

Two bus exchange priority techniques stated in IEEE standard document are discussed : a serial technique and a parallel technique. The communication design concept of UCN #5,6 PCS system also is specified in this section.

### 2.1 Serial Priority Technique

This scheme is implemented with a daisy chain technique. The bus priority output (BPRO) of each master is linked to the bus priority input (BPRN) of the next lower priority master. The BPRN of the highest priority master in the serial chain shall either be always active or connected to central bus arbiter. Serial priority resolution is accomplished in the following manner. If a master requests control of the bus, it shall set its BPRO high, which in turn disables the BPRN of all lower priority masters.

### 2.2 Parallel Priority Technique

In the parallel scheme, the bus occupation is determined by a bus arbiter. This is a priority technique, which determines the next master by a fixed priority structure or some other mechanism for sequential allocation. The BPRQ lines are not used in the parallel allocation BPRN scheme. Note that the parallel and serial schemes are compatible and therefore can be combined and used together on the same bus.

### 2.3 Bus Rotating Arbitration scheme in UCN PCS

This scheme applied to the Ulchin 5 & 6 nuclear power plant is designed so that a total of 16 microprocessors are implemented through the bus of the A233 backplane. This uses the bus rotating arbitration design in order for a mater to claim the bus. In order for this to occur, the following three conditions should exist:

- The falling edge of BCLK
- Bus grant ownership
- High state of BUSY signal

An individual or multiple bus masters determines that bus access is required and asynchronously issues a bus request (BREQ #). The bus masters then execute wait states until the above three conditions are achieved. The bus arbiter receives the bus request(s) and issues a bus priority in (BPRN #) for only one master based on the current highest priority requestor. At this point a combination of events must occur for an individual bus master to take control of the bus. The bus master with the bus grant signal will take the bus and indicate this by taking the bus BUSY low.

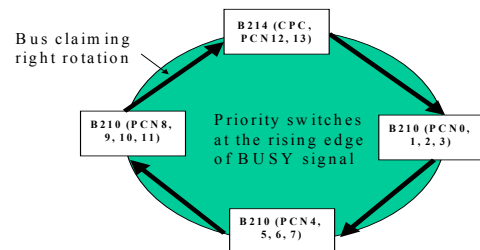


Figure 1. Bus Rotating Arbitration Scheme

In the bus rotating priority scheme (see Figure 1), the priority starts with the B214 PCB board. The B214 will get the bus grant if it requests. It will then occupy the bus by pulling the BUSY signal low when the falling edge of the bus clock occurs. If the B214 card releases the bus, the priority switches to B210 Links 0-3. Then, the bus arbiter in the Complex Programmable Logic Device (CPLD) will issue a bus grant to this highest priority card if it requests. This B210 Link 0-3 card will eventually occupy the bus at the falling edge of the bus clock after it gets the bus grant. Thu bus priority rotation occurs when the bus BUSY signal is rising to reach the threshold value

### 2.4 Fixed Priority Scheme

In the fixed priority scheme (see Figure 2), the priority would be fixed in the following fashion if this scheme were applied to the bus control of the CM of the UCN 5 & 6 PCS system.

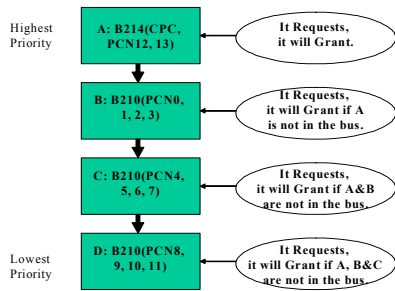


Figure 2. The Fixed Priority

In this approach, the bus arbiter won't use the threshold voltage of the BUSY signal to decide priority switch. The priority is fixed. For example, B214 has the highest priority. B210 PCN 11 has the lowest priority. The lower priority processors cannot get into the bus when the higher priority processors are on the bus. The lower priority processors can claim the bus when all of the higher priority processors have released the bus.

### 3. Bus Accessing Performance Evaluation

The bus accessing evaluation tests were performed with the bus rotating arbitration scheme versus the fixed priority scheme at the PCS test bed. PCN 0 wrote 110 bytes to the public memory of the CM and PCN 0 and 1 read back these bytes. Similar write/read was tested simultaneously for PCS 4 and 5, PCN 10 and 11, and PCN 12 and 13. The write/read was performed 100 times per ICL scan cycle. This test was conducted for a 14-days period per each scheme.

Figure 3 was plotted using the data logged from the bus rotating arbitration scheme and the fixed priority scheme respectively. As we compare the data of the two schemes, we observe the following.

- 1) For PCN Links 0-1, fixed priority loses 5% of bus accessing capability compared to the bus rotating arbitration scheme.
- 2) For PCN Links 10-11, fixed priority gains 8% of bus accessing capability against the bus rotating arbitration scheme.
- 3) For PCN Links 4-5 and 10-11, fixed priority loses 4% of bus accessing capability against the bus rotating arbitration scheme.

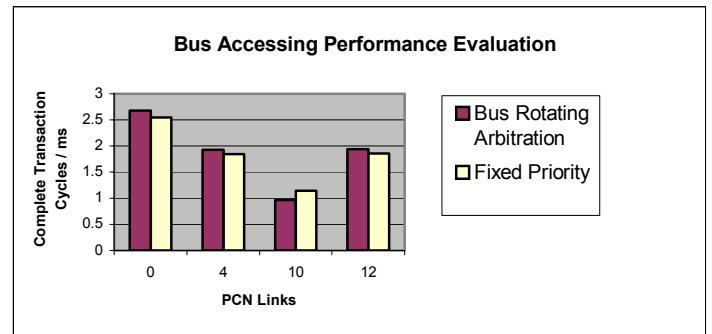


Figure 3. Bus Rotating Arbitration vs. Fixed Priority

### 4. Conclusion

As shown in figure 3 above, bus accessing capability between the two schemes does not make any significant difference. This means either scheme is able to be applied to UCN 5 & 6 PCS. However, to apply a particular scheme to nuclear power plant, sufficient tests and field proven history are absolutely necessary. Even though the fixed priority scheme provides even smoother bus activities as a result of the evaluation, the adoption of an unproven scheme to the field should be handled very cautiously.

### REFERENCES

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