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Testing of FBD including Timer Function Blocks

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1. Introduction

Testing for time-related behaviors of PLC software is important and should be performed carefully. This work focuses on testing of Function Block Diagram(FBD), one of the most widely used standard PLC programming languages.

In the previous case [1], functional testing on FBD has been done on the intermediate C source code transformed from an FBD network. We propose a structural testing method for FBD including timer function blocks without having to generate the intermediate code. In order to test a unit FBD, [2] transforms a unit FBD into a flowgraph based on several templates and apply existing structural testing techniques to the flowgraph. However, it did not address how timer function blocks could be tested. In this paper, we extend work reported in [2] by defining flowgraph segment templates corresponding to the timer function blocks.

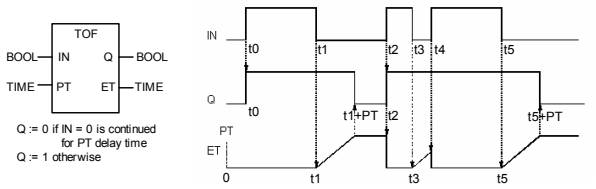
To demonstrate the effectiveness of the proposed method, we use a trip logic of Bistable Processor(BP) at Reactor Protection System(RPS) in Digital Plant Protection System(DPPS) which is being developed at Korea Nuclear Instrumentation and Control System R&D Center(KNICS) [3] in Korea as a case study.

2. Flowgraph Generation Template for Timer Function Block

An FBD network includes functions and function blocks. A function block has defined set of variables for internal storage and temporary data as well as input and output variables [5], while a function has no internal variables. All functions are transformed into one out of 3 types of flowgraph segments – a node, if-then-else, or switch structure – as proposed in [2].

According to the international standard IEC 61131-3[4], timer group includes function blocks such as TOF, TON and TP. Figure 1 represents TOF(Off Delay) function block and its behavioral defnition described by timing diagram. In this paper, we describe template generation process of TOF function block. Templates for TON and TP can be generated similarly.

TOF function block outputs *Q* as 0 when input *IN* is kept as 0 during the delay time *PT* since input *IN* changed from 1 to 0. Otherwise, the output *Q* is 1.



(a) (b)

Figure 1. TOF function block and its behavioral definition

To transform TOF into a flowgraph segment, we represent the behavior of TOF as the condition and action table. We identify the internal variables of TOF as *preIN*, the value of *IN* in the previous scan cycle, and the internal timer *inT* based on the timing diagram definition of TOF. To describe the behavior of TOF completely as conditions and actions, we need to specify all possible cases of related variables.

Variables affecting the condition are *preIN*, *IN*, and *inT*. There are 12 different conditions for combination of these three variables because the *preIN* and *IN* are Boolean and the domain of *inT* can be divided into 3 equivalent classes - [0,0], (0,*PT*), [*PT*,∞) - in the aspect of evaluation result of the condition. Table 1 shows a part of condition and action table of TOF.

Ca-ses	Condition			Action		Cases in figure 1(b)
	preIN	*IN*	*inT*	*Q*	*inT*	
b1	0	0	0	0	remains stopped	[0,t0)
b2	0	0	0<*inT*<*PT*	1	continues increasing	(t1,t1+*PT*), (t3,t4), (t5,t5+*PT*)
b3	0	0	*inT*>=*PT*	0	stops and remains	[t1+*PT*,t2), [t5+*PT*,-)
b4	0	1	0	1	stops and is reset	t0
b5	0	1	0<*inT*<*PT*	1	stops and is reset	t4

Table 1. A part of condition and action table to describe the behavior of TOF

Whole 12 pairs of condition and action can be reduced by logical combination of conditions for the same action. We define that two actions of TOF are identical if the values of *Q* and actions of *inT* are identical. We classified the actions of *inT* into 5 different cases: 'remains stopped', 'continues increasing', 'stops and remains', 'stops and is reset' and 'is reset and starts'. By combining conditions for the same action, the behavior of TOF can be described by 7 cases of conditions and actions. With this result, we make a

template for TOF function block. Figure 2 is a resulting template for TOF.

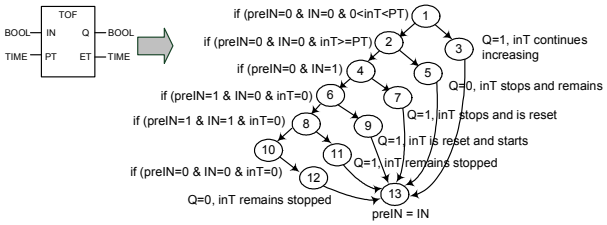


Figure 2. Template for TOF function block

3. FBD Unit Testing

3.1 Timer Function Block Testing

After transforming of a unit FBD into a flowgraph, we select proper test coverage criteria and generate satisfying set of test cases.

When a unit FBD includes only functions, one scan cycle testing is sufficient. On the other hand, correctness of the FBD networks containing timer function blocks cannot be tested in one cycle. In order to test timer function blocks, test cases must specify inputs covering multiple scan cycles and expected intermediate outputs at each scan cycle. We address intermediate (and internal) states as preconditions associated with each test case. Precondition is combination of evaluations of internal variables of timer function blocks.

In order to achieve sufficient testing for FBD networks with timer function blocks, it is desired to generate test cases to cover combination of input variables and preconditions as much as possible.

3.2 Case Study

We applied the proposed approach to the BP trip logic of DPPS RPS, which is being developed at KNICS. We seeded four different errors into the unit FBD in figure 3 and transformed it into a flowgraph in figure 4. We applied control flow testing with the All-Edges coverage criteria and data flow testing with the All-Uses coverage criteria for the flowgraph. Table 2 represents a part of a set of test cases satisfying All-Uses coverage criteria. The seeded errors were all found by the applied method.

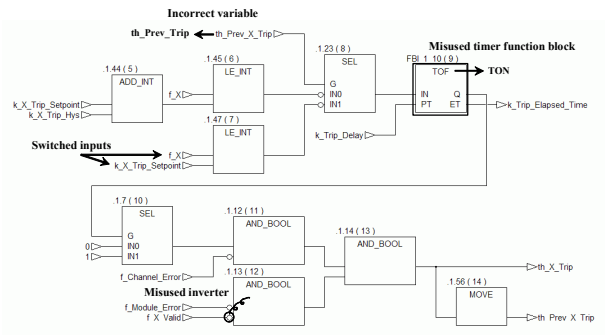


Figure 3. FBD for *th_Prev_X_Trip*

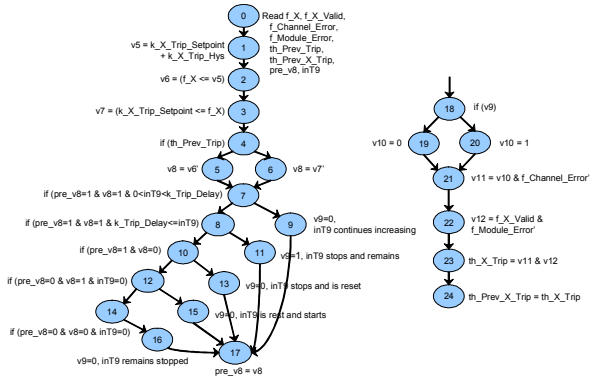


Figure 4. Flowgraph generated from the FBD unit for *th_Prev_X_Trip*

Test Cases	Precondition		Inputs						*th_Prev_X_Trip*	
	pre_v8	*inT9*	*PrevTr*	*PrevXTr*	*fX*	*CE*	*ME*	*Vld*	Ac.	Ex.
DT1	0	0	0	0	91	0	0	1	0	0
DT2	0	0	1	0	100	0	0	1	0	1
DT3	0	0	0	0	100	0	0	1	0	1
DT4	1	50	0	0	80	0	0	1	0	1
DT5	0	0	0	0	80	1	1	1	0	0

Table 2. A part of a set of test cases satisfying All-Uses test coverage criteria

4. Conclusion

We proposed a structural testing technique on Function Block Diagram(FBD) networks including timer function blocks. We presented how to generate transformation templates for the timer function blocks. After generating a flowgraph from an FBD network based on the several templates, we applied existing structural testing techniques for the generated flowgraph. We could confirm the effectiveness of the proposed method by applying it to industrial sample programs. By the proposed method, systematic structural testing for the FBD including timer function blocks became possible while there was no structural testing method for them before. We have a plan to support FBD testing automation and to extend this research to cover the integration testing issue.

REFERENCES

[1] http://www.framatome-anp.com

[2] E. Jee, J. Yoo, S. Cha, Control and Data Flow Testing on Function Block Diagrams, The 24th International Conference on Computer Safety, Reliability and Security (SAFECOMP 2005), LNCS 3688, pp.67-80, Fredrikstad, Norway, Sep. 28-30, 2005

[3] KNICS, Korea Nuclear Instrumentation and Control System Research and Development Center, http://www.knics.re.kr

[4] IEC, International Standard for Programmable Controllers: Programming Languages (Part 3), 1993

[5] R. Lewis, Programming industrial control systems using IEC 1131-3 Revised Edition(IEE Control Engineering Series), The Institute of Electrical Engineers, 1998