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An integration testing for the PLD(Programmable Logic Device) of a processor module

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1. Introduction

The PLD (Programmable Logic Device) module is a component of a processor module. The PLD contains the logic which interfaces with other hardware and software. These functions have been developed with a hardware logic structure previously, but now are being developed using VHDL (Very High Definition Language).
The regulation requirements define this VHDL code as a software, recommend that it must satisfy the software life cycle activities. NLCPU-1Q is a processor module PLD that is being developed following a software life cycle process in KNICS (Korea Nuclear I&C System) project.
This paper describes the items related to an integration testing of development life cycle for NLCPU-1Q. The functions, testing process, testing environment and testing procedure of the NLCPU-1Q are included in detail.

2. The Function of NLCPU-1Q

NLCPU-1Q PLD interfaces with CPU's peripheral devices such as Memory, RTC, UART, LED, and Watchdog Timer. The functions of NLCPU-1Q are as follows:

- Chip Selector signal generation
- Access cycle wait signal generation
- Piggyback Connector interface
- Watchdog Timer interface
- RTC(Real Time Clock) interface
- UART interface
- LED interface
- Switch interface
- Reset signal generation
- Interrupt generation
- Power module interface

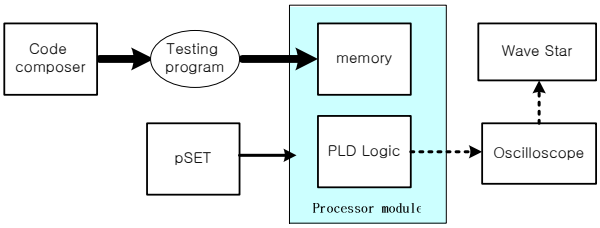
3. The process of integration testing

To perform an integration test for the PLD logic, test cases are generated. These cases were generated from the requirement specifications and the design specifications of the PLD. Figure1 shows the method to input and output the data for an integration test. A testing input data is loaded into the CPU through two methods as follows:

- Testing program of processor module
- Interrupt signal using pSET tool

First, the method to perform the PLD functions using a testing program is follows:

1. The program to access integrated target hardware is created by Code Composer tool
2. After compiling the program, the execution file is downloaded into a processor module. Run the execution file
3. Confirm that the PLD outputs the signal to control peripheral hardware

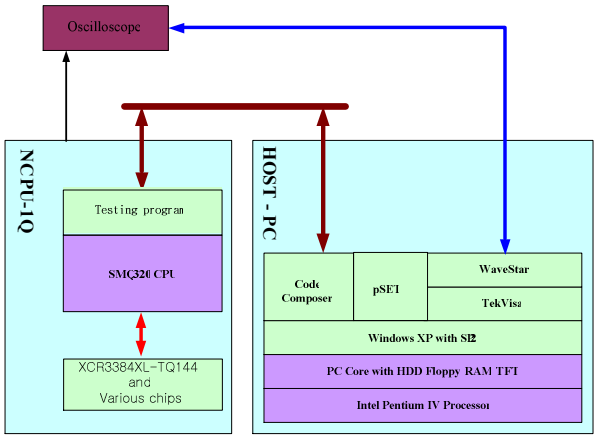


[Figure1] Testing method

Second, the method to test an interrupt function of the PLD is performed by using the pSET tool.

4. Testing Environment

The environment for an integration test of the PLD logic is shown in Figure2.



[Figure2] Testing environment

Software resources necessary for the integration testing are Windows XP, Code Composer, pSET,

TekVisa, and WaveStar. Code Composer creates the testing program and downloads the executing files. pSET is used to generate the interrupt signal. TekVisa and WaveStar support the oscilloscope, read the measurement data, and display the results. Hardware resources used for the integration testing are a bus module, a power module, a processor module, an oscilloscope and emulator to operate the processor module. Host PC is also needed.

5. Integration testing procedure

The test cases for PLD are shown in Table1, where Input, expected output and the test results are described.

[Table1] Test Case Chart

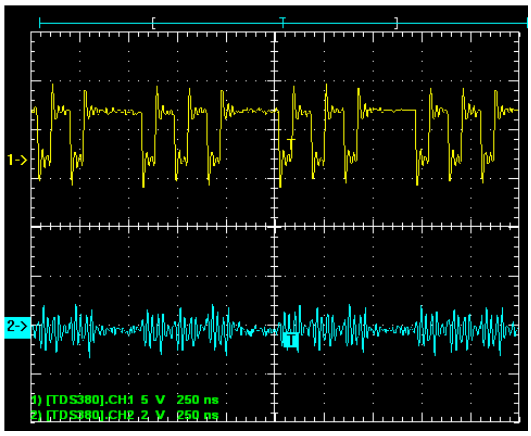
No	Input	Expect value	result	P/F
	Inputvar1, inputvar2	outputvar1, outputvar2		
1	value, value	expect value1, expect value2	result1, result2	
2	value, value	expect value1, expect value2	result1, result2	
3	value, value	expect value1, expect value2	result1, result2	

To assign the testing data into variables, the testing program must be created. Because the PLD program was downloaded in ROM of PLD after being compiled, the source code is not changed. Therefore, a testing program which can access integrated targets is created. For example, the testing program to integrate with the FLASH memory is made as follows:

```
var1 = *(unsigned int *)0xE00000;
var2 = *(unsigned int *)0x200001;
*(unsigned int *)0xEFFFFF = data;
```

This program is written and is compiled using Code Composer tool. Execution file is loaded into the region of the operating system of a processor module and executed. The procedure to verify the excepted value is as follows:

1. Connect pins of PLD which outputs the interface signal of hardware device to oscilloscope.
2. Confirm the output signal using oscilloscope.
3. Compare if the result is the same as the expected output



[Figure3] The result signal from oscilloscope

6. Conclusion

The integration test of NLCPU-1Q PLD has been performed to verify whether the functions in the requirement specifications are operated correctly or not. The major functions of the PLD are the Chip Selector Signal Generation, the Access Cycle Wait Generation, the Interrupt and Reset Signal Generation, and the Interface with Peripheral Device. To confirm that these functions are operated correctly, a testing program was created and the results have been acquired.

The PLD based on VHDL only performs a simulation because of regarding to simple hardware logic previously. We measured the real signal in the PLD and verified directly that the functions of PLD are being performed correctly.

REFERENCES

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